

PRODUCT SPECIFICATION

MODEL: JCB101IPS-42A

<◇>PRELIMINARY SPECIFICATION

<◆>APPROVAL SPECIFICATION

| CUSTOMER<br>APPROVED | DESIGNED | CHECKED | APPROVED |
|----------------------|----------|---------|----------|
|                      |          |         |          |

| SUPPLIER<br>APPROVED | DESIGNED | CHECKED | APPROVED |
|----------------------|----------|---------|----------|
|                      |          |         |          |

# 深圳市晶彩世界科技有限公司

## REVISION STATUS

| Version | Revise Date | Page | Content       | Modified by |
|---------|-------------|------|---------------|-------------|
| V1.0    | 2019.07.02  | -    | First Issued. | CYZ         |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |
|         |             |      |               |             |

# 深圳市晶彩世界科技有限公司

| Contents                        | Page |
|---------------------------------|------|
| 1.0. General Specification      | 4    |
| 2.0. Absolute Maximum Ratings   | 5    |
| 3.0. Optical characteristics    | 6    |
| 4.0. Block diagram              | 10   |
| 5.0. Interface pin connection   | 12   |
| 6.0. Electrical characteristics | 14   |
| 7.0. Reliability test items     | 19   |
| 8.0. Outline dimension          | 20   |
| 9.0. Bom List                   | 21   |
| 10.0. Lot mark                  | 22   |
| 11.0. Package specification     | 23   |
| 12.0. General Precaution        | 24   |
|                                 |      |

# 深圳市晶彩世界科技有限公司

## 1.0 GENERAL DESCRIPTION

### 1.1 Introduction

The model JCB101IPS-42A is a color active matrix thin film transistor (TFT) liquid crystal display without plagiarizer. This model is composed of amorphous silicon TFT as a switching device. This TFT LCD has a 10.1-inch wide (16:9) diagonally measured active display area with WVGA (1024 horizontal by 600 vertical pixel) resolution. Each pixel is divided into Red, Green, Blue dots which are arranged in vertical stripes.

### 1.2 Features

- 10.1 inch configuration.
- 16.7M color by 8 bit R.G.B. signal input
- RoHS/Halogen Free Compliance

### 1.3 Applications

- Mobile NB
- Digital Photo frame
- Display terminal for AV application

### 1.4 General information

| Item              | Specification             | Unit     |
|-------------------|---------------------------|----------|
| Screen Size       | 10.1 inches               | Diagonal |
| Number of Pixel   | 1024 RGB (H) ×600(V)      | Pixels   |
| Display area      | 222.72(H) x 125.28(V)     | mm       |
| Outline Dimension | 235.0 x 143.0 x 4.50(Typ) | mm       |
| Display mode      | Normally Black            | --       |
| Pixel arrangement | RGB Vertical stripe       | --       |
| Pixel pitch       | 0.2175(H) ×0.2088(V)      | mm       |
| Back-light        | LED Side-light type       | --       |
| Surface treatment | Anti - glare              | --       |
| Interface         | LVDS                      |          |

# 深圳市晶彩世界科技有限公司

## 1.5 Mechanical Information

| Item        |                | Min.  | Typ.  | Max.  | Unit |
|-------------|----------------|-------|-------|-------|------|
| Module Size | Horizontal (H) | 234.8 | 235.0 | 235.2 | mm   |
|             | Vertical (V)   | 142.8 | 143.0 | 143.2 | mm   |
|             | Depth (D)      | 4.30  | 4.50  | 4.70  | mm   |
| Weight      |                | --    | TBD   | --    | g    |

## 2.0 ABSOLUTE MAXIMUM RATINGS

### 2.1 Electrical Absolute Rating

#### 2.1.1 TFT LCD Module

| Item                 | Symbol | Min  | Max   | Unit | Note   |
|----------------------|--------|------|-------|------|--------|
| Power supply voltage | VDD    | -0.5 | 3.96  | V    | GND=0  |
|                      | AVDD   | --   | 14.85 | V    | AGND=0 |

#### Note:

1. Stresses above those listed under” Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at indicated in the operational sections(6.1) of this specification.

2. Ta=25±2℃

### 2.2 Environment Absolute Rating

| Item                  | Symbol           | Min. | Max. | Unit | Note |
|-----------------------|------------------|------|------|------|------|
| Storage temperature   | T <sub>STG</sub> | -30  | 80   | ℃    |      |
| Operating temperature | T <sub>OPR</sub> | -20  | 70   | ℃    |      |

**Note:** If users use the product out off the environmental operation range(temperature and humidity), it will have visual quality concerns.

# 深圳市晶彩世界科技有限公司

## 3.0 OPTICAL CHARACTERISTICS

### 3.1 Optical specification

| Item                                |       | Symbol                          | Condition                                 | Min   | Type  | Max   | Unit | Note      |
|-------------------------------------|-------|---------------------------------|-------------------------------------------|-------|-------|-------|------|-----------|
| White luminance<br>(Center)         |       | YL                              | Θ=0<br><br>Normal<br><br>Viewing<br>Angle | --    | 500   | TBD   | nits | (1)(4)(6) |
| Response time                       |       | T <sub>r</sub> + T <sub>f</sub> |                                           | --    | 30    | 40    | msec | (1)(3)    |
| Contrast ratio                      |       | CR                              |                                           | --    | 800   | --    | --   | (1)(2)    |
| Color<br>Chromaticity<br>(CIE 1931) | white | W <sub>x</sub>                  |                                           | 0.260 | 0.310 | 0.360 |      | (1)(4)    |
|                                     |       | W <sub>y</sub>                  | 0.280                                     | 0.330 | 0.380 |       |      |           |
| Viewing Angle                       | Hor.  | Θ <sub>L</sub>                  | CR≥10                                     | 80    | 85    | --    |      | (1)(4)    |
|                                     |       | Θ <sub>R</sub>                  |                                           | 80    | 85    | --    |      |           |
|                                     | Ver.  | Θ <sub>U</sub>                  |                                           | 80    | 85    | --    |      |           |
|                                     |       | Θ <sub>D</sub>                  |                                           | 80    | 85    | --    |      |           |
| Brightness                          |       | B <sub>UNI</sub>                | Θ=0                                       | 70    | 80    | --    | %    | (5)       |
| Color gamut (NTSC)                  |       | S                               |                                           | --    | 50    | --    | %    | C-light   |
| Optima View Direction               |       | ALL VIEW                        |                                           |       |       |       |      |           |

- 1), 客户签样亮度 $\pm 10\%$  = 大货亮度, 小于10%视为不良。
- 2), 大货同一批色调一致的情况下(目视同为冷色或暖色)与客户签样相比, X色坐标相差 $\pm 0.015$ , Y色坐标相差 $\pm 0.02$ 以内视为正常OK品。

### 3.2 Measuring Condition

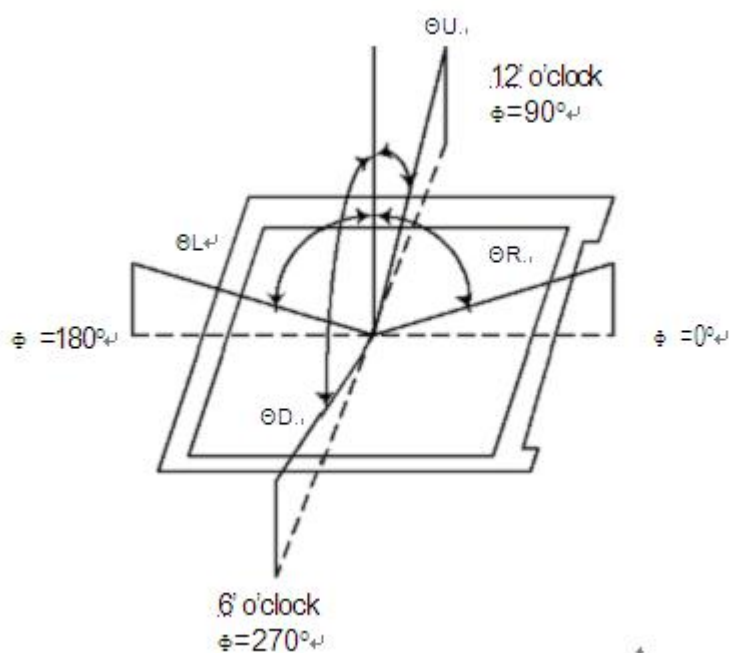
- Measuring surrounding: dark room
- LED current IL: 180mA
- Ambient temperature:  $25 \pm 2^\circ\text{C}$
- 30min. warm-up time

### 3.3 Measuring Equipment

- BM-7 optical characteristics.
- Measuring spot size: 20 ~ 21mm

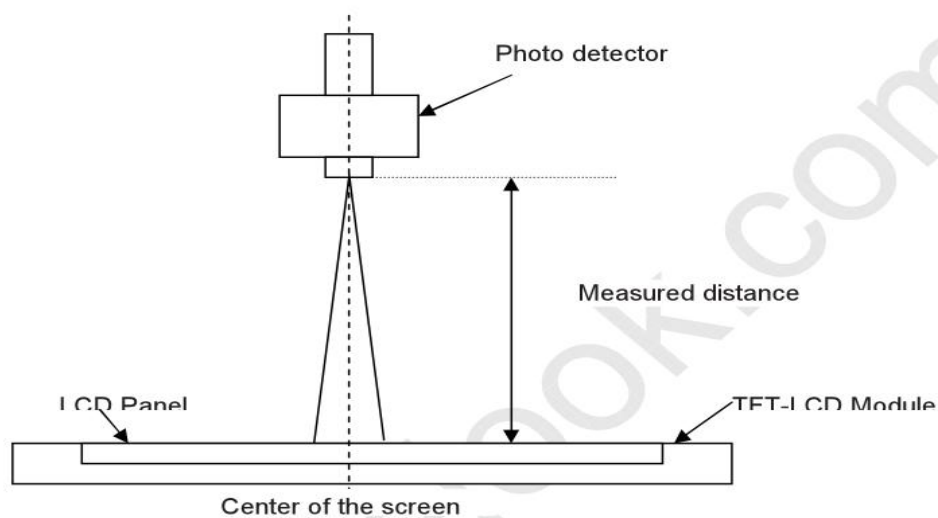
**Note (1) Definition of Viewing angle range:**

Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

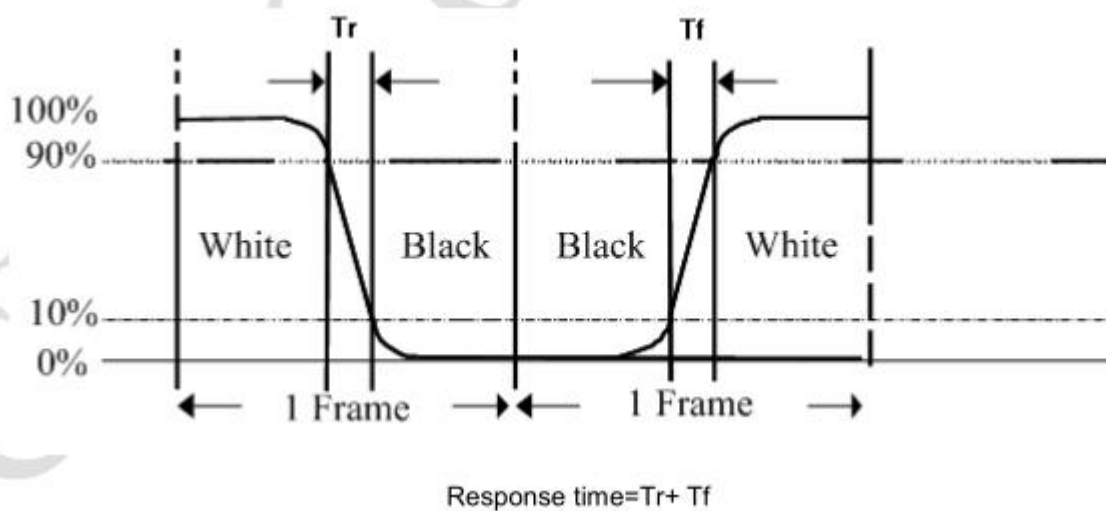


**Note (2) Definition of Contrast Ratio(CR):** Measured at the center point of panel

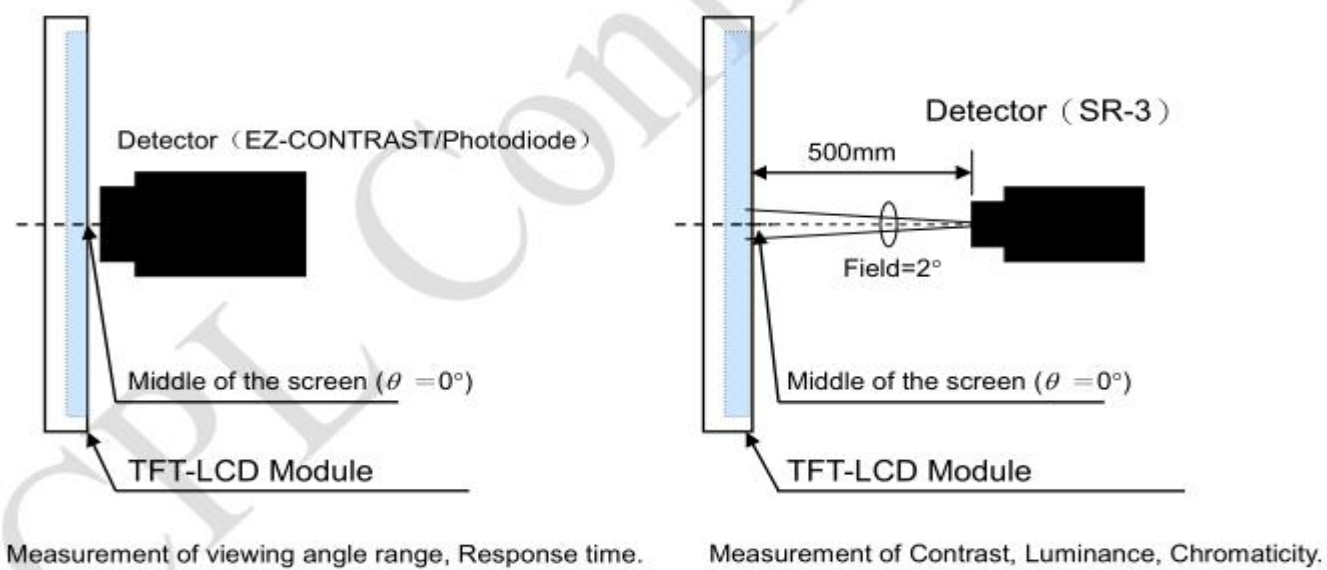
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$



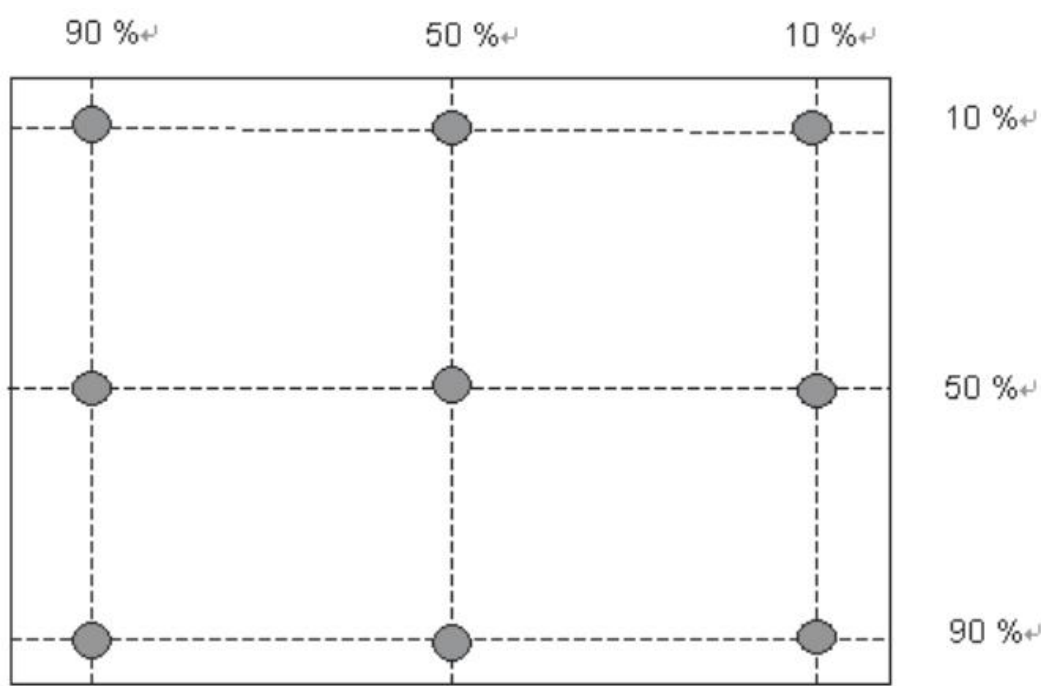
**Note (3) Definition of Response Time: Sum of  $T_R$  and  $T_F$**



**Note (4) Definition of optical measurement setup**



**Note (5) Definition of brightness uniformity**



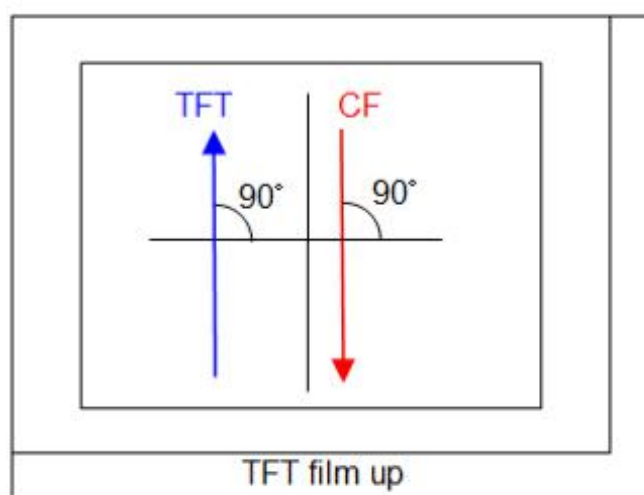
# 深圳市晶彩世界科技有限公司

---

$$\text{Luminance uniformity} = \frac{(\text{Min Luminance of 9 points})}{(\text{Max Luminance of 9 points})} \times 100 \%$$

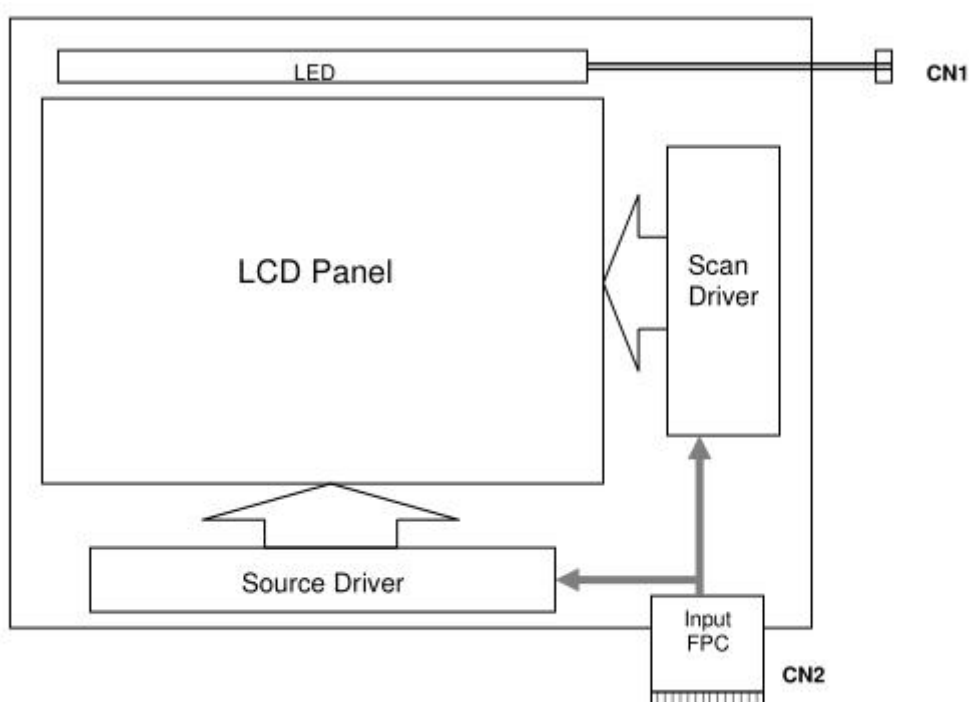
---

**Note (6) Rubbing Direction** (The different Rubbing Direction will cause the different optima view direction).

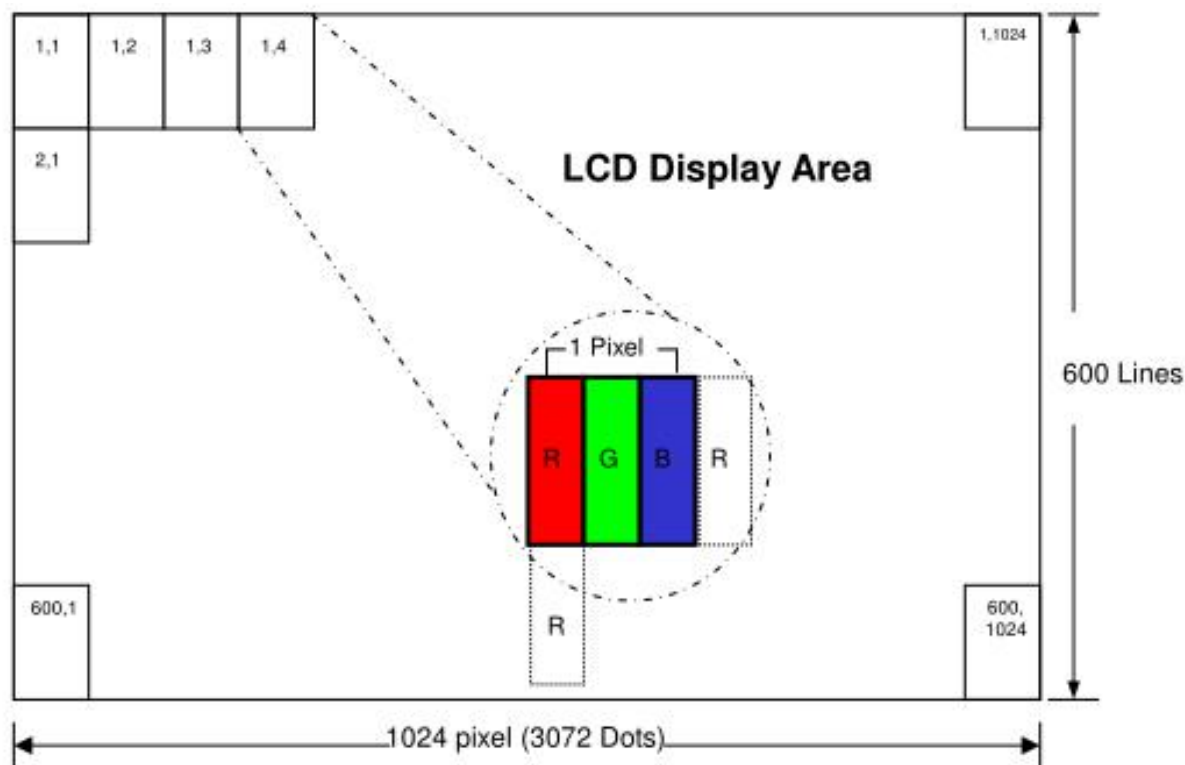


## 4.0 BLOCK DIAGRAM

### 4.1 TFT LCD Module



4.2 Pixel Format



5.0 INTERFACE PIN CONNECTION

5.1 TFT LCD Module: FPC UP Connector, (FH28-60S-0.5H (HIROSE), 60pin,pitch = 0.5mm)

| Pin No. | Symbol | Function                 | Remark |
|---------|--------|--------------------------|--------|
| 1       | AGND   | Analog ground            |        |
| 2       | AVDD   | Power for Analog Circuit |        |
| 3       | VDD    | Digital Power            |        |
| 4       | GND    | Power ground             |        |
| 5       | VCOM   | Common Voltage           |        |
| 6       | VDD    | Digital Power            |        |
| 7       | GND    | Power ground             |        |
| 8       | NC     | No connection            |        |
| 9       | NC     | No connection            |        |
| 10      | NC     | No connection            |        |
| 11      | NC     | No connection            |        |
| 12      | NC     | No connection            |        |
| 13      | NC     | No connection            |        |
| 14      | NC     | No connection            |        |

# 深圳市晶彩世界科技有限公司

|    |          |                                                                                                                                                          |       |
|----|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 15 | GND      | Power ground                                                                                                                                             |       |
| 16 | VDD_LVDS | LVDS Power                                                                                                                                               |       |
| 17 | GND      | Power ground                                                                                                                                             |       |
| 18 | PIND3    | Positive LVDS differential data inputs                                                                                                                   |       |
| 19 | NIND3    | Negative LVDS differential data inputs                                                                                                                   |       |
| 20 | GND      | Power ground                                                                                                                                             |       |
| 21 | PINC     | Positive LVDS differential clock inputs                                                                                                                  |       |
| 22 | NINC     | Negative LVDS differential clock inputs                                                                                                                  |       |
| 23 | GND      | Power ground                                                                                                                                             |       |
| 24 | PIND2    | Positive LVDS differential data inputs                                                                                                                   |       |
| 25 | NIND2    | Negative LVDS differential data inputs                                                                                                                   |       |
| 26 | GND      | Power ground                                                                                                                                             |       |
| 27 | PIND1    | Positive LVDS differential data inputs                                                                                                                   |       |
| 28 | NIND1    | Negative LVDS differential data inputs                                                                                                                   |       |
| 29 | GND      | Power ground                                                                                                                                             |       |
| 30 | PIND0    | Positive LVDS differential data inputs                                                                                                                   |       |
| 31 | NIND0    | Negative LVDS differential data inputs                                                                                                                   |       |
| 32 | GND      | Power ground                                                                                                                                             |       |
| 33 | GND_LVDS | LVDS ground                                                                                                                                              |       |
| 34 | RESET    | Global reset pin. Active low to enter reset state.<br>Suggest to connecting with RC reset circuit for stability.<br>Normally pull high. (R=10KΩ、C=0.1uF) | Note1 |

| Pin No. | Symbol | Function                                                                                                                                                  | Remark |
|---------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| 35      | STBYB  | Standby mode, Normally pulled high<br>STBYB = "1", normal operation<br>STBYB = "0", timing controller, source driver will turn off, all output are High-Z |        |
| 36      | NC     | No connection                                                                                                                                             |        |
| 37      | VDD    | Digital Power                                                                                                                                             |        |
| 38      | NC     | No connection                                                                                                                                             |        |
| 39      | AGND   | Analog ground                                                                                                                                             |        |
| 40      | AVDD   | Power for Analog Circuit                                                                                                                                  |        |
| 41      | VCOM   | Common Voltage                                                                                                                                            |        |
| 42      | NC     | No connection                                                                                                                                             |        |
| 43      | GND    | Power ground                                                                                                                                              |        |
| 44      | VDD    | Digital Power                                                                                                                                             |        |
| 45      | GND    | Power ground                                                                                                                                              |        |
| 46      | NC     | No connection                                                                                                                                             |        |
| 47      | NC     | No connection                                                                                                                                             |        |
| 48      | NC     | No connection                                                                                                                                             |        |
| 49      | NC     | No connection                                                                                                                                             |        |

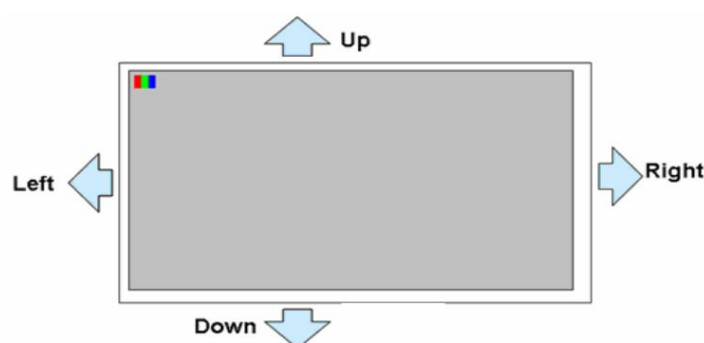
# 深圳市晶彩世界科技有限公司

|    |         |                                                                |  |
|----|---------|----------------------------------------------------------------|--|
| 50 | NC      | No connection                                                  |  |
| 51 | NC      | No connection                                                  |  |
| 52 | NC      | No connection                                                  |  |
| 53 | GND     | Power ground                                                   |  |
| 54 | VDD     | Digital Power                                                  |  |
| 55 | SELB    | 6bit/8bit mode select<br>DINT=1:8-bit(Default)<br>DINT=0:6-bit |  |
| 56 | VGH     | Positive power for TFT                                         |  |
| 57 | VDD     | Digital Power                                                  |  |
| 58 | VGL     | Negative power for TFT                                         |  |
| 59 | GND     | Power ground                                                   |  |
| 60 | NC/BIST | No connection                                                  |  |

Note1: Global reset pin: Active low to enter reset mode. Suggest connecting with an RC reset circuit for stability.

Normally pull high. (R=10K $\Omega$ , C=0.1 $\mu$ F)

Note: If RC is not added, users must follow the rule, T2 > 15ms on page 18 item 6.5 power on/off sequence.



## 5.2 Back-Light Unit

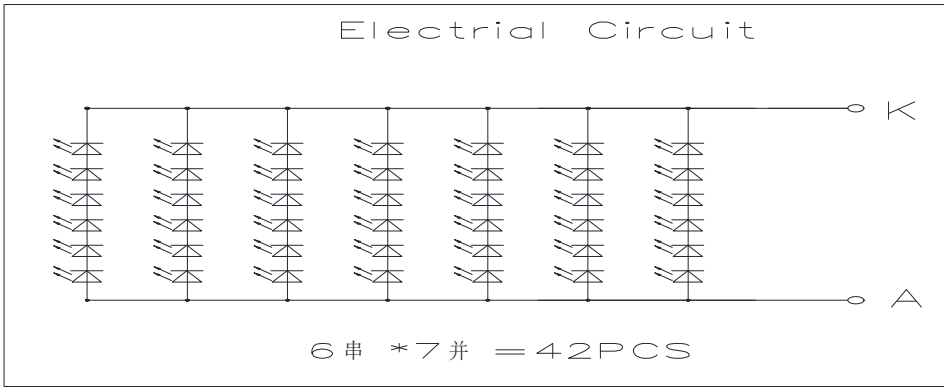
The backlight system is an edge-lighting type with 6C \* 7P=42 LED.

The characteristics of the LED are shown in the following tables.

| Item                    | Symbol | Min   | Typ   | Max  | Unit | Note |
|-------------------------|--------|-------|-------|------|------|------|
| LED current             | IL     | 160   | 180   | 200  | mA   |      |
| LED voltage             | VL     | 17.0  | 19.2  | 21.0 | V    |      |
| Operating LED life time | Hr     | 20000 | 25000 | --   | Hour | (1)  |

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 $\pm$ 3  $^{\circ}$ C , typical IL value indicated in the above table and the fL=50k Hz until the brightness becomes less than 50%.

# 深圳市晶彩世界科技有限公司



## 6.1 TFT LCD Module

| Item                                 | Symbol | Min. | Typ. | Max. | Unit | Note                |
|--------------------------------------|--------|------|------|------|------|---------------------|
| Digital Power Supply Voltage For LCD | DVDD   | 3.0  | 3.3  | 3.6  | V    |                     |
| Analog Power Supply Voltage          | AVDD   | 8.5  | 9.6  | 10.5 | V    | 调整对比度，调大颜色变深，调小颜色变浅 |
| Gate On Power Supply Voltage         | VGH    | 17.0 | 18.0 | 19.0 | V    |                     |
| Gate Off Power Supply Voltage        | VGL    | -6.5 | -6.0 | -5.5 | V    |                     |
| Common Power Supply Voltage          | VCOM   | 3.1  | 3.2  | 3.3  | V    | Note 1              |
| Operation frequency                  | FCLK   | —    | —    | 200  | KHZ  |                     |

**Note 1:** Please adjust VCOM to make the flicker level be minimum. Typ VCOM 电压值  
只做参考，具体以实际效果为准（根据FLICKER 状态可调整）

**Note (2):** Be sure to apply the power Voltage as the power sequence spec.

**Note (3):** GND=0V

## 6.2 Input Timing Table(For 1024RGB x 600 panel)

# 深圳市晶彩世界科技有限公司

## DE mode

| Parameter                       | Symbol   | Value |      |      | Unit |
|---------------------------------|----------|-------|------|------|------|
|                                 |          | Min.  | Typ. | Max. |      |
| DCLK frequency @Frame rate=60hz | fclk     | 40.8  | 51.2 | 67.2 | Mhz  |
| Horizontal display area         | thd      | 1024  |      |      | DCLK |
| HSYNC period time               | th       | 1114  | 1344 | 1400 | DCLK |
| HSYNC blanking                  | thb+thfp | 90    | 320  | 376  | DCLK |
| Vertical display area           | Tvd      | 600   |      |      | H    |
| VSYNC period time               | Tv       | 610   | 635  | 800  | H    |
| VSYNC blanking                  | Tvb+Tvfp | 10    | 35   | 200  | H    |

## HV mode

### Horizontal input timing

| Parameter                       | Symbol | Value        |              |            | Unit |
|---------------------------------|--------|--------------|--------------|------------|------|
| Horizontal display area         | thd    | 1024         |              |            | DCLK |
| DCLK frequency@ Frame rate=60hz | fclk   | Min.<br>44.9 | Typ.<br>51.2 | Max.<br>63 | Mhz  |
| 1 Horizontal Line               | th     | 1200         | 1344         | 1400       | DCLK |
| HSYNC pulse width               | Min.   | 1            |              |            |      |
|                                 | Typ.   | —            |              |            |      |
|                                 | Max.   | 140          |              |            |      |
| HSYNC blanking                  | thb    | 160          | 160          | 160        |      |
| HSYNC front porch               | thfp   | 16           | 160          | 216        |      |

## HV mode

### Vertical input timing

| Parameter             | Symbol | Value |      |      | Unit |
|-----------------------|--------|-------|------|------|------|
|                       |        | Min.  | Typ. | Max. |      |
| Vertical display area | tvd    | 600   |      |      | H    |
| VSYNC period time     | tv     | 624   | 635  | 750  | H    |
| VSYNC pulse width     | tvpw   | 1     | —    | 20   | H    |
| VSYNC back porch      | tvb    | 23    | 23   | 23   | H    |
| VSYNC front porch     | tvfp   | 1     | 12   | 127  | H    |

## 6.3 AC Electrical Characteristics

# 深圳市晶彩世界科技有限公司

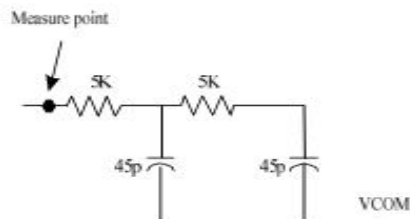
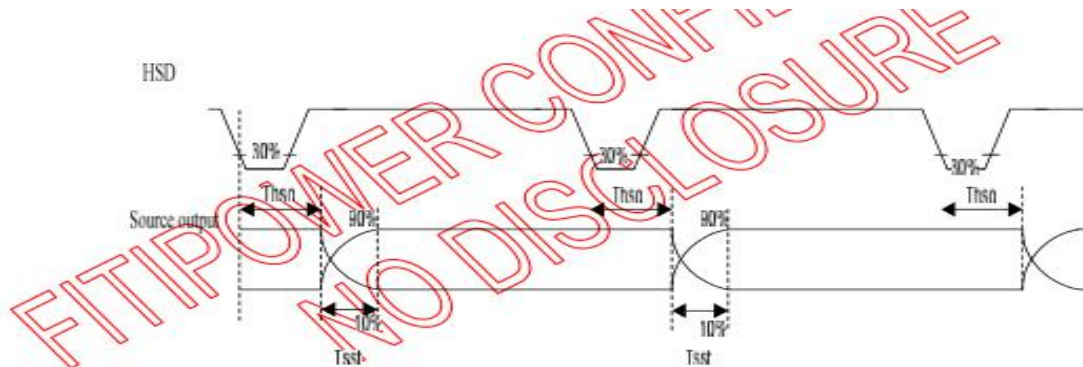
(TA = -20 to 85° C, VDD = 2.3 to 3.6V, AVDD = 8 to 13.5V, GND = AGND = 0V)

TTL mode

| Parameter              | Symbol | Condition                                                  | Min. | Typ. | Max. | Unit |
|------------------------|--------|------------------------------------------------------------|------|------|------|------|
| VDD Power On Slew rate | TPOR   | From 0V to 90% VDD                                         | -    | -    | 20   | ms   |
| RSTB pulse width       | TRST   | DCLK = 65MHz                                               | 50   | -    | -    | us   |
| DCLK cycle time        | Tcph   | -                                                          | 14   | -    | -    | ns   |
| DCLK pulse duty        | Tcwh   | -                                                          | 40   | 50   | 60   | %    |
| VSD setup time         | Tvst   | -                                                          | 5    | -    | -    | ns   |
| VSD hold time          | Tvhd   | -                                                          | 5    | -    | -    | ns   |
| HSD setup time         | Thst   | -                                                          | 5    | -    | -    | ns   |
| HSD hold time          | Thhd   | -                                                          | 5    | -    | -    | ns   |
| Data set-up time       | Tdsu   | D0[7:0], D1[7:0], D2[7:0] to DCLK                          | 5    | -    | -    | ns   |
| Data hold time         | Tdhd   | D0[7:0], D1[7:0], D2[7:0] to DCLK                          | 5    | -    | -    | ns   |
| DE setup time          | Tesu   | -                                                          | 5    | -    | -    | ns   |
| DE hold time           | Tehd   | -                                                          | 5    | -    | -    | ns   |
| Output stable time     | Tsst   | 10% to 90% target voltage,<br>CL=90pF, R=10K ohm (Cascade) | -    | -    | 6    | us   |
|                        |        | Dual gate                                                  |      |      | 3    |      |

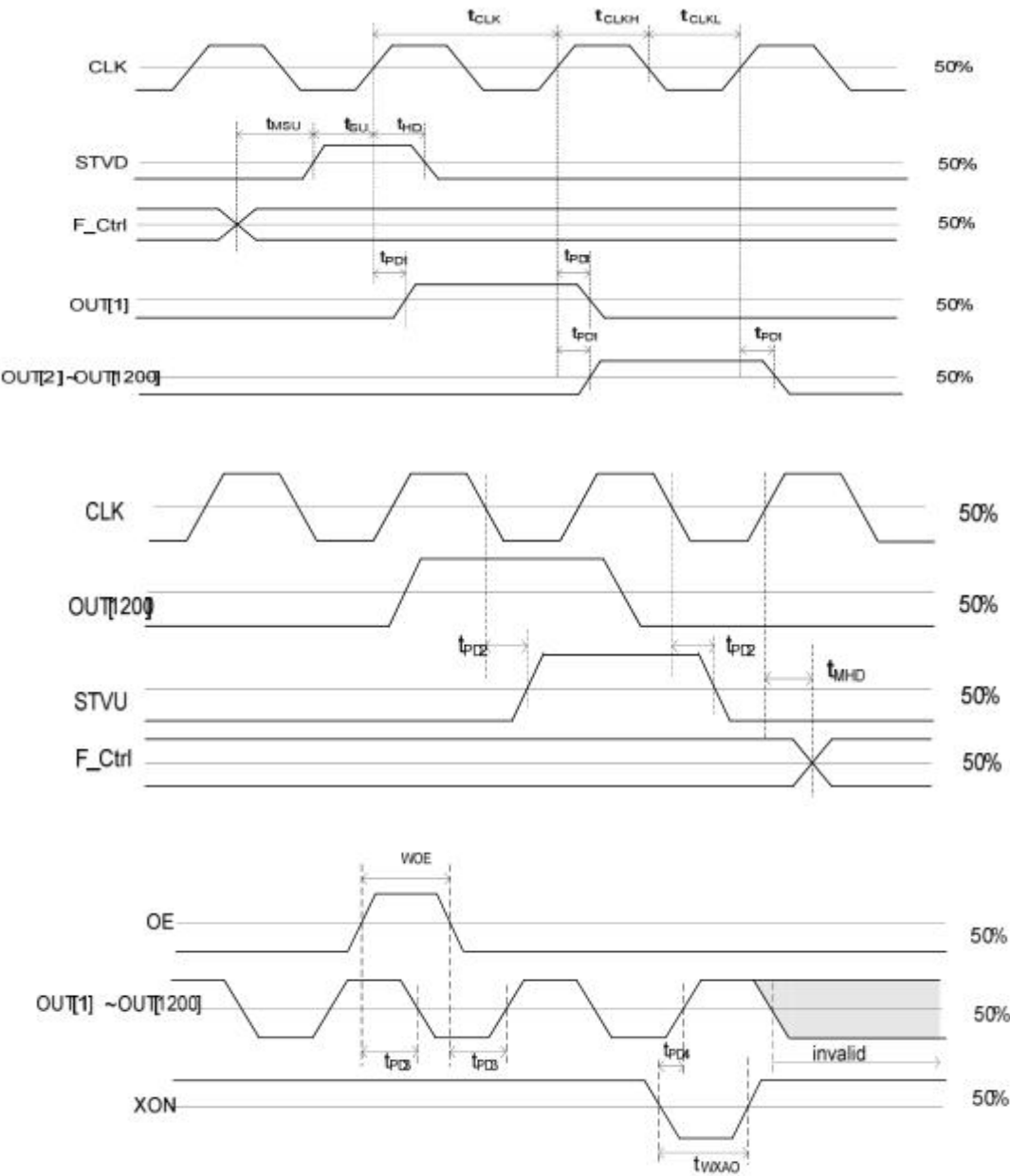
## Output Timing Table

| Parameter                      | Symbol | Min. | Typ. | Max. | Unit | Condition     |
|--------------------------------|--------|------|------|------|------|---------------|
| DCLK frequency                 | Fclk   | -    | 65   | 71   | MHz  | VDD =2.3~3.6V |
| DCLK cycle time                | Tclk   | 14.1 | 15.4 | -    | ns   |               |
| DCLK pulse duty                | Tcwh   | 40   | 50   | 60   | %    | Tclk          |
| Time from HSD to Source Output | Thso   | -    | 64   | -    | DCLK |               |
| Time from HSD to LD            | Thld   | -    | 64   | -    | DCLK |               |
| Time from HSD to STV           | Thstv  | -    | 2    | -    | DCLK |               |
| Time from HSD to CKV           | Thckv  | -    | 20   | -    | DCLK |               |
| Time from HSD to OEV           | Thoev  | -    | 4    | -    | DCLK |               |
| LD pulse width                 | Twld   | -    | 10   | -    | DCLK |               |
| CKV pulse width                | Twckv  | -    | 66   | -    | DCLK |               |
| OEV pulse width                | Twoev  | -    | 74   | -    | DCLK |               |

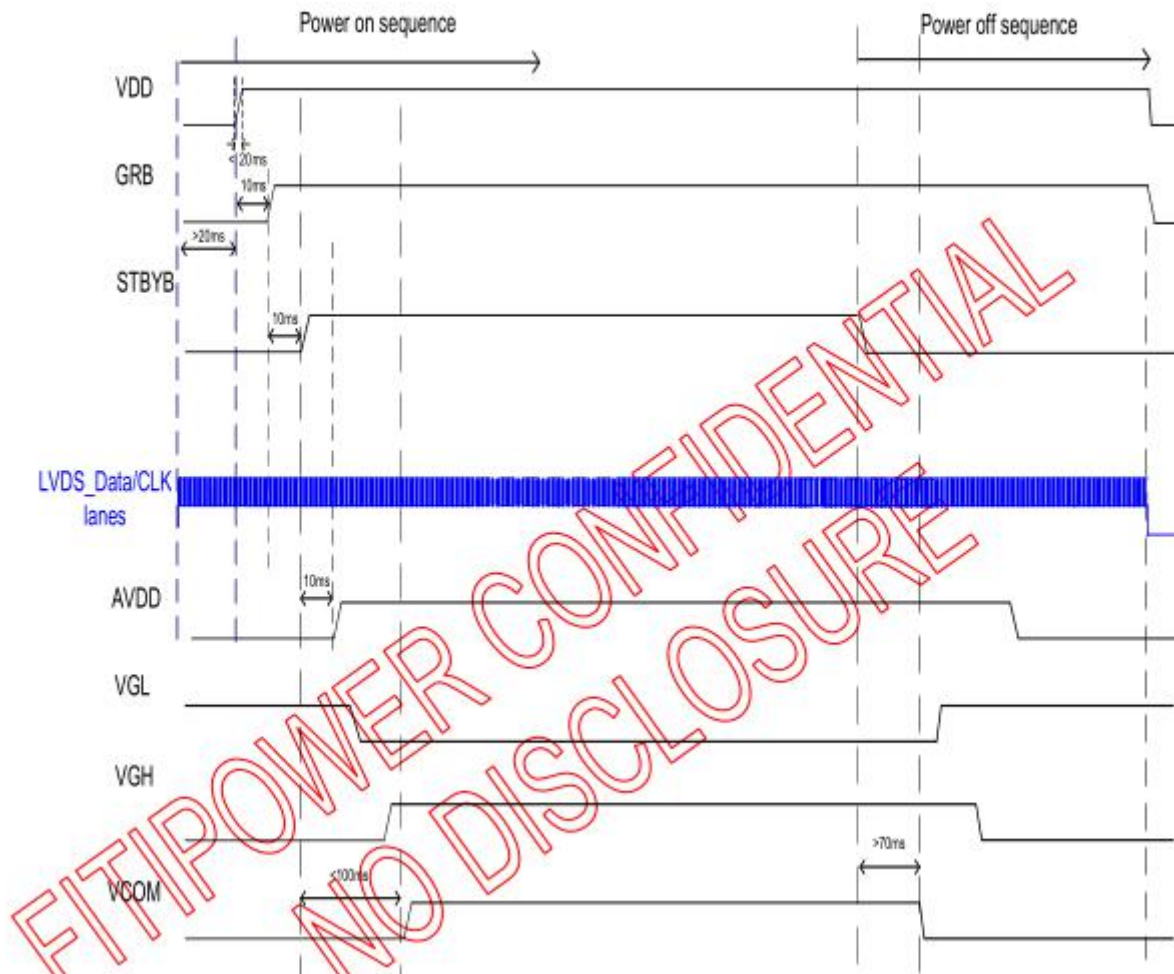


Source Output Timing(Cascade)

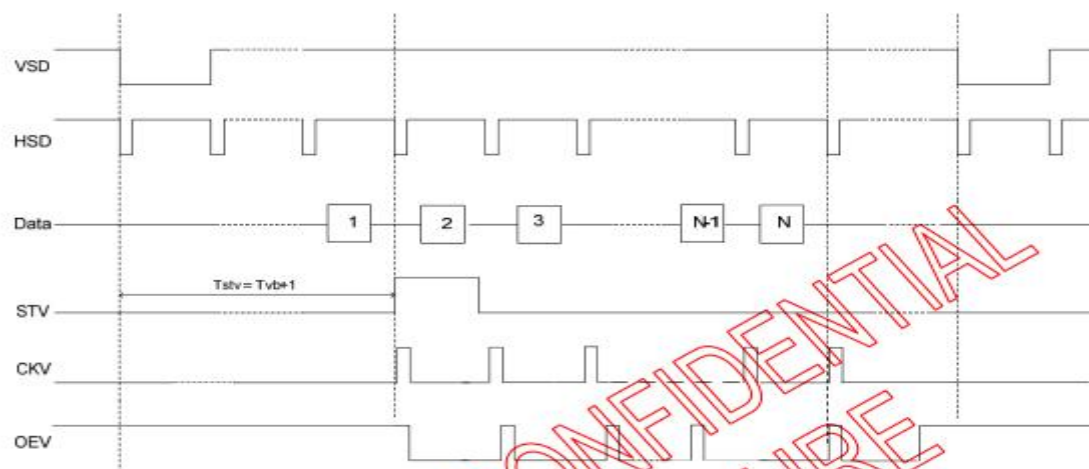
6.4 Timing Waveform



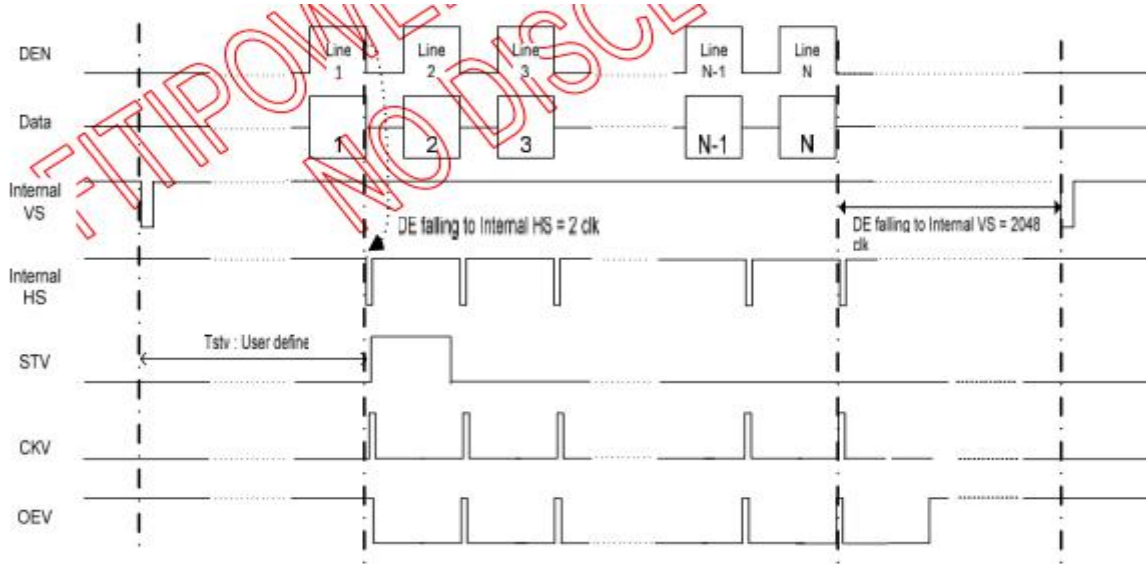
## 6.4.3 Power-On/Off Timing Sequence for LVDS Interface



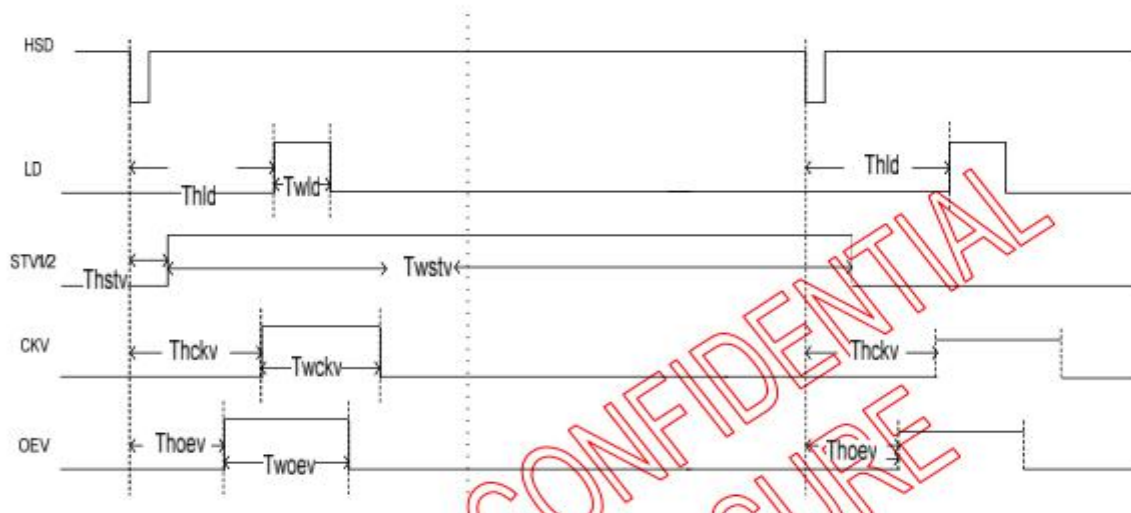
## 6.4.4 Vertical Timing Diagram HV mode(Cascade)



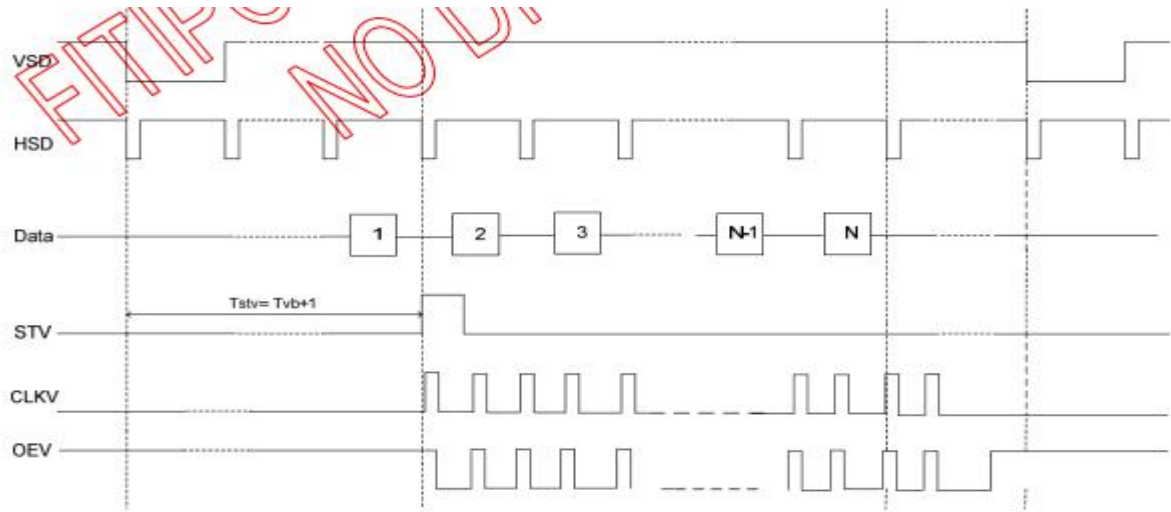
## 6.4.5 Vertical Timing Diagram DE mode(Cascade)



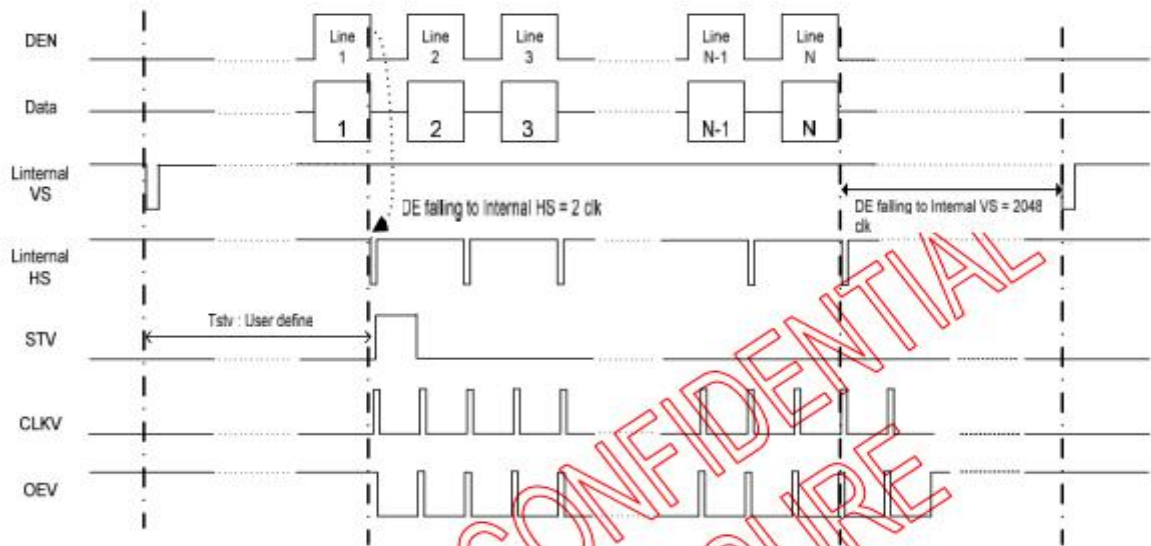
## 6.4.6 Gate output timing diagram(Cascade)



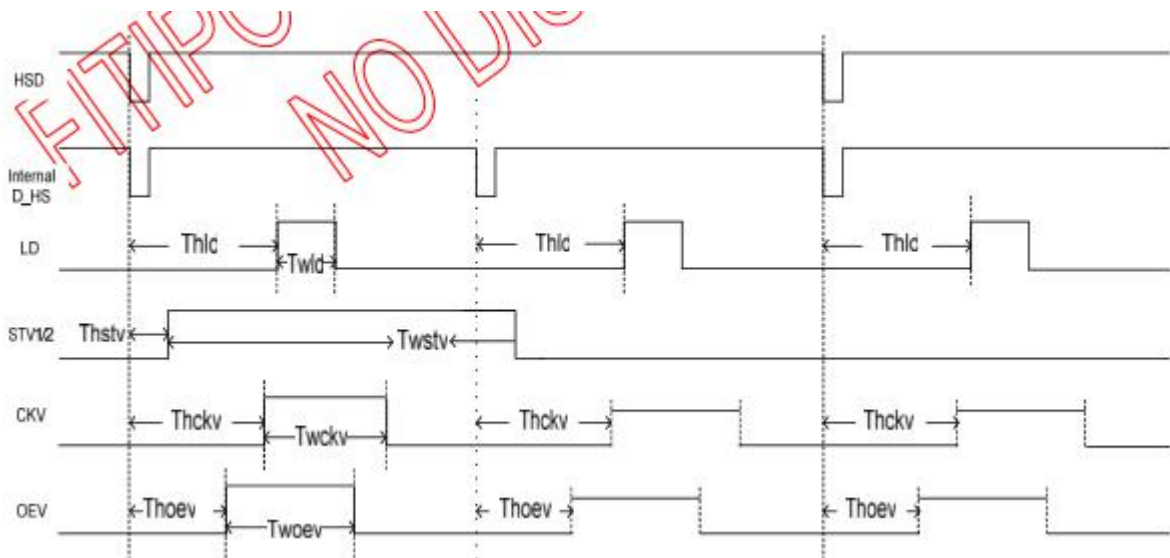
6.4.7Vertical Timing Diagram HV mode(Dual Gate)



6.4.8Vertical Timing Diagram DE mode(Dual Gate)



6.4.9Gate output timing diagram(Dual Gate)



# 深圳市晶彩世界科技有限公司

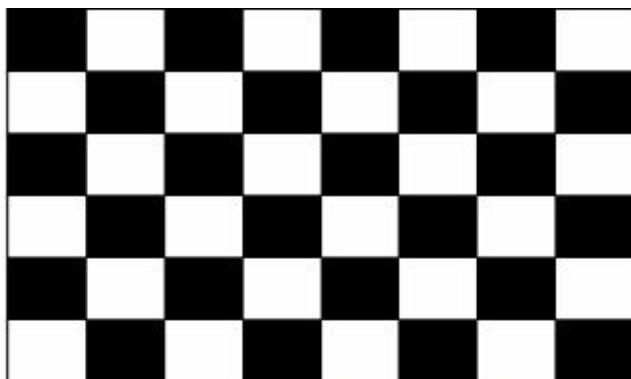
## 7.0 RELIABILITY TEST ITEMS

| No. | Test Item                                     | Conditions                                                                                                                                                                                                                                                          | Note |
|-----|-----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 1   | High Temperature Storage                      | Ta=+80℃, 12hrs                                                                                                                                                                                                                                                      |      |
| 2   | Low Temperature Storage                       | Ta=-30℃, 12hrs                                                                                                                                                                                                                                                      |      |
| 3   | High Temperature Operation                    | Ta=+70℃, 12hrs                                                                                                                                                                                                                                                      |      |
| 4   | Low Temperature Operation                     | Ta=-20℃, 12hrs                                                                                                                                                                                                                                                      |      |
| 5   | High Temperature and High Humidity(operation) | Ta=+60℃, 80%RH 24hrs                                                                                                                                                                                                                                                |      |
| 6   | Thermal cycling Test                          | -20℃/30 min ~ +70℃/30 min for a total 10cycles,<br>Start with cold temperature and end with high temperature.                                                                                                                                                       |      |
| 7   | Vibration Test<br>(Non-operation)             | <ul style="list-style-type: none"><li>● Frequency range:8~33.3Hz</li><li>● Stoke: 1.3 mm</li><li>● Vibration: sinusoidal wave, perpendicular axis(both x, z axis: 2hrs ,y axis: 4hrs).</li><li>● Sweep: 2.9G,33.3 Hz -400 Hz</li><li>● Cycle time: 15 min</li></ul> |      |
| 8   | Shock Test<br>(Non-operation)                 | <ul style="list-style-type: none"><li>● Shock level: 980m/s 2 (equal to 100G).</li><li>● Waveform: half sinusoidal wave,6ms.</li><li>● Number of shocks: ±X,±Y,±Z axes for a total of six shock inputs.</li></ul>                                                   |      |
| 9   | ESD Test                                      | 150pF, 330Ω, ±8kV&±15kV air& contact test                                                                                                                                                                                                                           | 1    |
|     |                                               | 200pF, 0Ω, ±200V contact test                                                                                                                                                                                                                                       | 2    |

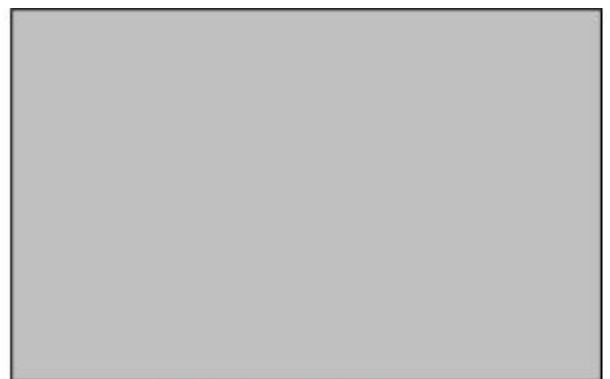
Note 1: LCD glass and metal bezel

Note 2: IF connector pins

Note 3: Operation with test pattern sustained for 4hrs, then change to gray pattern immediately.

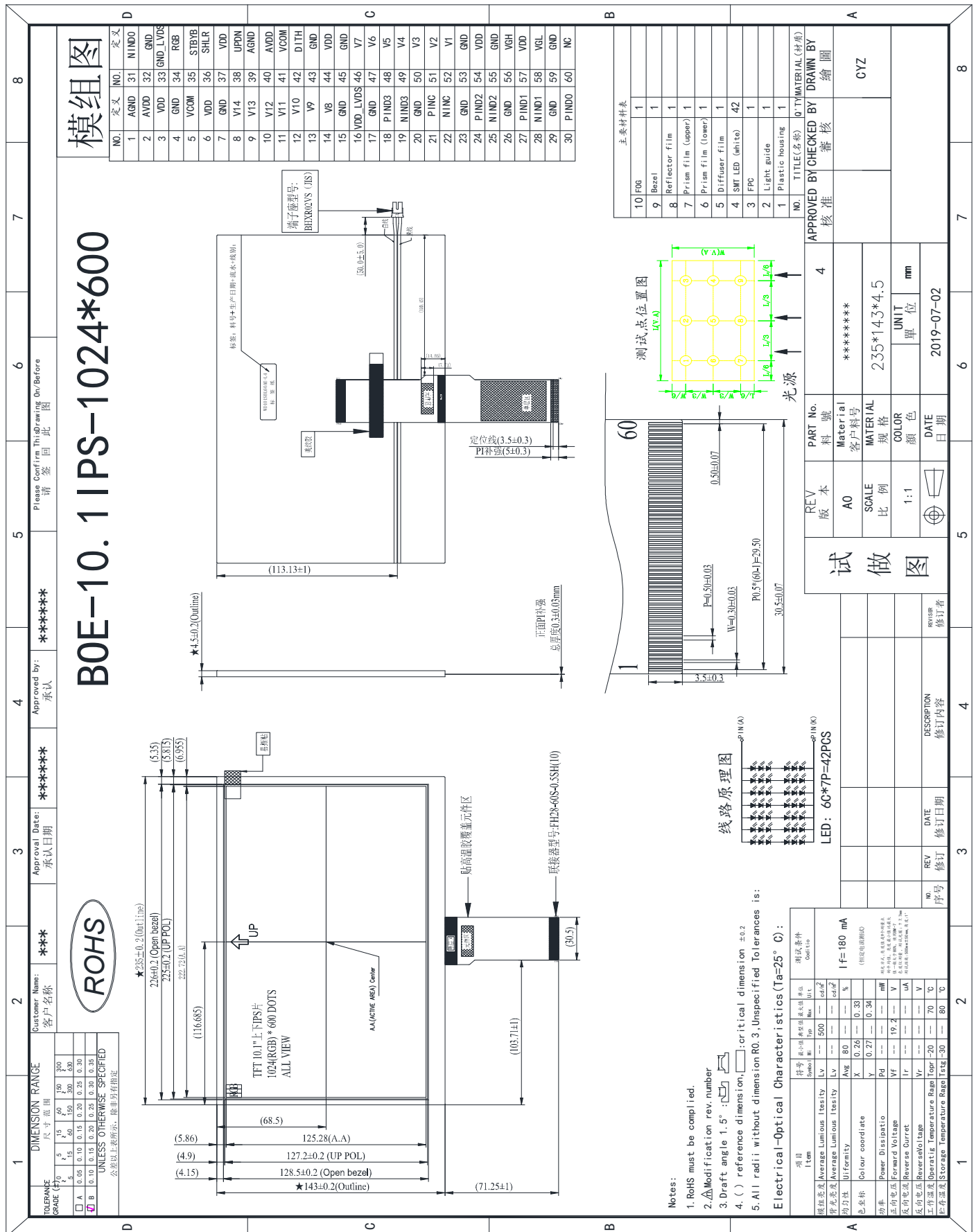


(a) Test Pattern (chess board Pattern )



(b) Gray Pattern

## 8.0 OUTLINE DIMENSION



# 深圳市晶彩世界科技有限公司

## 9.0 LOT MARK

### 9.1 Location of Lot Mark

- (1) Location: The label is attached to the backside of the LCD module.
- (2) Detail of the Mark: as attached below.
- (3) This is subject to change without prior notice.

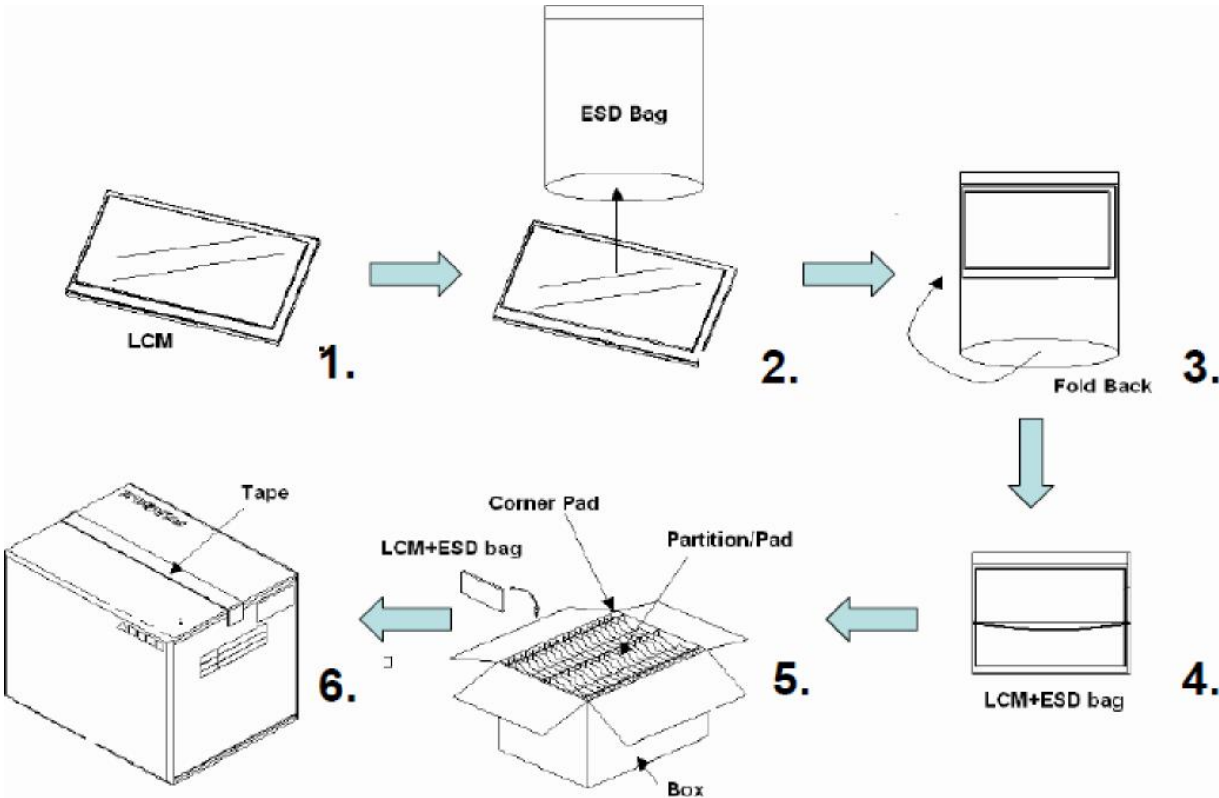
---T.B.D

## 10.0 PACKAGE SPECIFICATION

### 10.1 Packing form

| LCM Model | LCM Qty. in the box | Inner Box Size ( mm ) | Note |
|-----------|---------------------|-----------------------|------|
|           | 50 pcs/box          | 455±5 x 305±5 x 205±5 |      |

### 10.2 Packing assembly drawings



| Items         | Material               | Notice   |
|---------------|------------------------|----------|
| Box           | Corrugated Paper Board | AB Flute |
| Partition/Pad | Corrugated Paper Board | B Flute  |
| Corner Pad    | Corrugated Paper Board | AB Flute |
| ESD bag       | PE                     |          |

## 11.0 GENERAL PRECAUTION

### 11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

### 11.2 Assembly Precaution

- 11.2.1 Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
- 11.2.2. Please design display housing in accordance with the following guide lines.
  - 11.2.2.1 Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
  - 11.2.2.2 Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
- 11.2.3 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands.(Polarizer film, surface of LCD panel is easy to be flawed.)
- 11.2.4 Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module, If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
- 11.2.5 Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
- 11.2.6 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
- 11.2.7 Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

### 11.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. Century does not warrant the module, if customers disassemble or modify the module.

### 11.4 Breakage of LCD Panel

- 11.4.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
- 11.4.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.
- 11.4.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
- 11.4.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

## 11.5 Absolute Maximum Ratings and Power Protection Circuit

- 11.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
- 11.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- 11.5.3. It's recommended to employ protection circuit for power supply.

## 11.6 Operation

- 11.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
- 11.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
- 11.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
- 11.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
- 11.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

## 11.7 Static Electricity

- 11.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
- 11.7.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.
- 11.7.3 Persons who handle the module should be grounded through adequate methods.

## 11.8 Disposal

When disposing LCD module, obey the local environmental regulations.

## 11.9 Others

- 11.9.1 A strong incident light into LCD panel might cause display characteristics' changing inferior because of Polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land Strong UV rays.
- 11.9.2 Please pay attention to a panel side of LCD module not to contact with other materials in pressing it alone.
- 11.9.3 For the packaging box, please pay attention to the followings:
  - 11.9.3.1 Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
  - 11.9.3.2 Please do not pile them up more than 6 boxes(They are not designed so) And please do not turn over.
  - 11.9.3.3 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
  - 11.9.3.4 Packing box and inner case for LCDs are made of cardboard, So please pay attention not to get them wet(Such like keeping them in high humidity or wet place can occur getting them wet.)