

深圳市晶彩世界科技有限公司

PRODUCT SPECIFICATION

MODEL: JCB090IPS - 36A

<◇>PRELIMINARY SPECIFICATION

<◆>APPROVAL SPECIFICATION

CUSTOMER APPROVED	DESIGNED	CHECKED	APPROVED

SUPPLIER APPROVED	DESIGNED	CHECKED	APPROVED

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REVISION STATUS

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1. GENERAL DESCRIPTION

1.1 Introduction

BOE Display model JCB090IPS - 36A is a color active matrix thin film Transistor(TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a Switching device. This model is composed of a TFT LCD panel,a driving circuit and a back light system.This TFT LCD has a 7(16:9) inch diagonally measured active display area with WSVGA (1024 horizontal by 600 vertical pixel) Resolution.

1.2 Features

- 9 inch (16:9 diagonal) configuration
- 16.7M color by 8 bit + Hi -FRC input
- RoHS/Halogen Free Compliance

1.3 Applications

- Automotive

1.4 TFT LCD General information

Item	Specification		Unit
Outline Dimension	210.7x126.5 x5.1 (typ)		mm
Display area	196.608(H) x114.5(V)		mm
Number of pixel	1024 RGB (H) x 600(V)		pixels
Pixel pitch	0.192 (H) x 0.19025(V)		mm
Pixel arrangement	RGB Vertical stripe		
Display mode	Normally black		
NTSC	50 (typ.)		%
Surface treatment	Antiglare with IPS Flim		
Weight	(146)g (Typ.)		g
Back-light	White LED		
Power Consumption	Logic	0.5(Max) @ Black pattern .Frame rate 60Hz	W
	BL System	2.3(typ) @ Black pattern w/o LED driver	W

1.5 Mechanical information

Item	Min.	Typ.	Max.	unit
Module size	Horizontal(H)	210.5	210.7	mm
	Vertical(V)	126.3	126.5	mm
	Depth(D)	---	5.1	mm
weight	----	(146)	---	g

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2. MECHANICAL SPECIFICATION

9.0 IPS 1024*600 模组图

D PIN DEFINITION

Pin	Assignment	Pin Assignment	Assignment
1	GND	31	RJ11NO-
2	VDD	32	GND
3	VDD	33	GND
4	GND	34	RESET
5	VCOM	35	SYBY6
6	VDD	36	SCLR
7	GND	37	VDD
8	V14	38	UPDN
9	V13	39	GND
10	V12	40	VDD
11	V11	41	VDD
12	V10	42	DITH
13	V9	43	GND
14	V8	44	VDD
15	GND	45	GND
16	VDD	46	V7
17	GND	47	V6
18	RX03+	48	V5
19	RX03-	49	V4
20	GND	50	V3
21	RXC01N+	51	V2
22	RXC01N-	52	V1
23	GND	53	GND
24	RXIN2+	54	VDD
25	RXIN2-	55	SELB
26	GND	56	VGH
27	RXIN1+	57	VDD
28	RXIN1-	58	VGL
29	GND	59	GND
30	RXIN0+	60	NC/OUT

B 主要材料表

10	P60	1	
9	Bezel	1	
8	Reflector film	1	
7	Prism film (upper)	1	
6	Prism film (lower)	1	
5	Baffles film	1	
4	SMT LED (white)	36	
3	FPC	1	
2	Light guide	1	
1	Plastic housing	1	

C 测试点位置图

A 线路原理图

LED: 6*6=36 PCS

DETAIL A (4:1)

Notes:

1. ROHS must be complied.
2. Modification rev. number
3. Draft angle 1.5° : □□□
4. () reference dimension, □□□ : critical dimension □□□
5. All radii without dimension R0.3, unspecified tolerances is.

Electrical-Optical Characteristics (Ta=25°C) :

项目	条件	参数	单位	测试条件	
模组亮度	Average Luminous Intensity	Iv	450 ~ 500	cd/m ²	
	Average Luminous Intensity	Iv	—	cd/m ²	
均匀性	均匀度	Agg	75	%	
	Color coordinate	X	0.26	0.33	
色彩	Power Dissipation	Pd	—	W	
	正向电压	Vf	117.4	V	17.4
反向电流	反向电压	Vr	—	V	1M
	反向电流	Ir	—	mA	100
工作温度	工作温度	Top	-20 ~ 70	℃	-20 ~ 70
	储存温度	Tstg	-30 ~ 80	℃	-30 ~ 80

LED: 6*6=36 PCS

试做图

REV	版本	PART NO.	REV	Part No.	Material	料號	APPROVED BY	CHECKED BY	DATE DRAWN BY
A0									

A

SCALE	比例	UNIT	量位	mm
1:1				

修订内容
序号
REV
修订日期
DESCRIPTION

修订者
REVISER
DATE
DATE

日期
DATE
日期
DATE

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3. PIN DESCRIPTION

Lvds Connector HRS Model Number :FH33-60S-0.5SH

No.	Symbol	Function	Remark
1	AGND	Analog ground	
2	AVDD	Power for Analog Circuit	
3	VDD	Digital Power	
4	GND	Power ground	
5	VCOM	Common Voltage	
6	VDD	Digital Power	
7	GND	Power ground	
8	NC	No connection	
9	NC	No connection	
10	NC	No connection	
11	NC	No connection	
12	NC	No connection	
13	NC	No connection	
14	NC	No connection	
15	GND	Power ground	
16	VDD_LVDS	LVDS Power	
17	GND	Power ground	
18	PIND3	Positive LVDS differential data inputs	
19	NIND3	Negative LVDS differential data inputs	
20	GND	Power ground	
21	PINC	Positive LVDS differential clock inputs	
22	NINC	Negative LVDS differential clock inputs	
23	GND	Power ground	
24	PIND2	Positive LVDS differential data inputs	
25	NIND2	Negative LVDS differential data inputs	
26	GND	Power ground	
27	PIND1	Positive LVDS differential data inputs	
28	NIND1	Negative LVDS differential data inputs	
29	GND	Power ground	
30	PIND0	Positive LVDS differential data inputs	
31	NIND0	Negative LVDS differential data inputs	
32	GND	Power ground	

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33	GND_LVDS	LVDS ground	
34	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with RC reset circuit for stability. Normally pull high.(R=10KΩ, C=0.1uF)	
35	STBYB	Standby mode, Normally pulled high STBYB = "1", normal operation STBYB = "0", timing controller, source driver will turn off, all output are High-Z	
36	NC	No connection	
37	VDD	Digital Power	
38	NC	No connection	
39	AGND	Analog ground	
40	AVDD	Power for Analog Circuit	
41	VCOM	Common Voltage	
42	DITH	Dithering function enable control.Normally pull low. DITHER = "1" , LVDS input data is 8 bits DITHER = "0" , LVDS input data is 6 bits	
43	GND	Power ground	
44	VDD	Digital Power	
45	GND	Power ground	
46	NC	No connection	
47	NC	No connection	
48	NC	No connection	
49	NC	No connection	
50	NC	No connection	
51	NC	No connection	
52	NC	No connection	
53	GND	Power ground	
54	VDD	Digital Power	
55	SELB	6bit/8bit mode select DINT=0:8-bit DINT=1:6-bit(Default)	
56	VGH	Positive power for TFT	
57	VDD	Digital Power	
58	VGL	Negative power for TFT	
59	GND	Power ground	
60	NC/BIST	No connection	

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4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	5.0	V
Analog supply voltage	AVDD	-0.3	15	V
Gate on voltage	VGH	-0.3	25	V
Gate off voltage	VHL	-20	0.3	V

4.2 TFT LCD MODULE

4.2.1 OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Supply Voltage	VDD	3.0	3.3	3.6	V
TFT Gate ON Voltage	VGH	-	18	-	V
TFT Gate OFF Voltage	VHL	-	-8	-	V
TFT Common electrode voltage	VCOM	3.6	4.0	4.6	V
Analog Power Supply voltage	AVDD	9.6	10.4	13.5	V

NOTE

4.3 Switching Characteristics for LVDS Receiver

Symbol	Item	Min.	Typ.	Max.	Unit	Remark
IVGH	Gate on current	--	1.0	--	mA	VGH=18V
IVGL	Gate OFF current	--	1.0	--	mA	VGL=-8V
IVDD	Digital Current	--	35	--	mA	VDD=3.3
IAVDD	Analog Power Supply voltage	--	70	--	mA	AVDD=10.2V
IVCOM	TFT Common electrode voltage	--	3	--	mA	VCOM=4.4V

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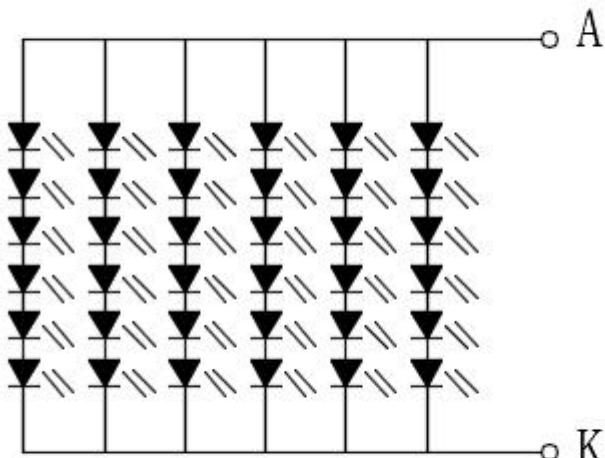
4.4 BACK LIGHT UNIT

T_a=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I _{LED}		160	180	mA	Total LED
Forward voltage	V _F	16	17	19.2	V	I _F =160mA
Reverse current	I _R			50	μA	V _R =5V,1LED
Power dissipation	P _d	2520			mW	Total LED
Peak forward current	I _{FP}	150			mA	1LED
Reverse Voltage	V _R	5			V	1LED

4.5 POWER ON/OFF SEQUENCE

线路原理图



LED: 6*6=36 PCS

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Power on timing sequenc

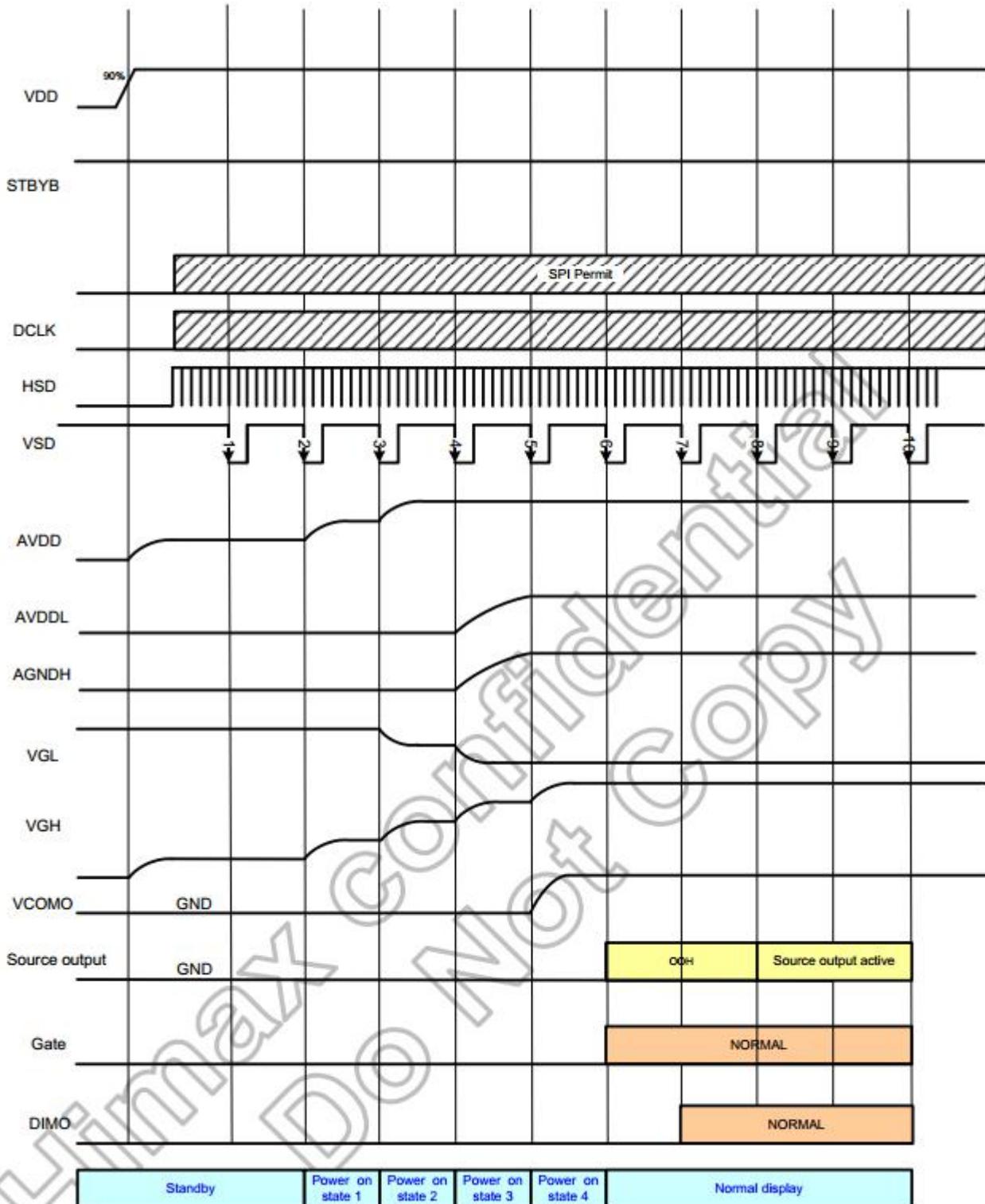
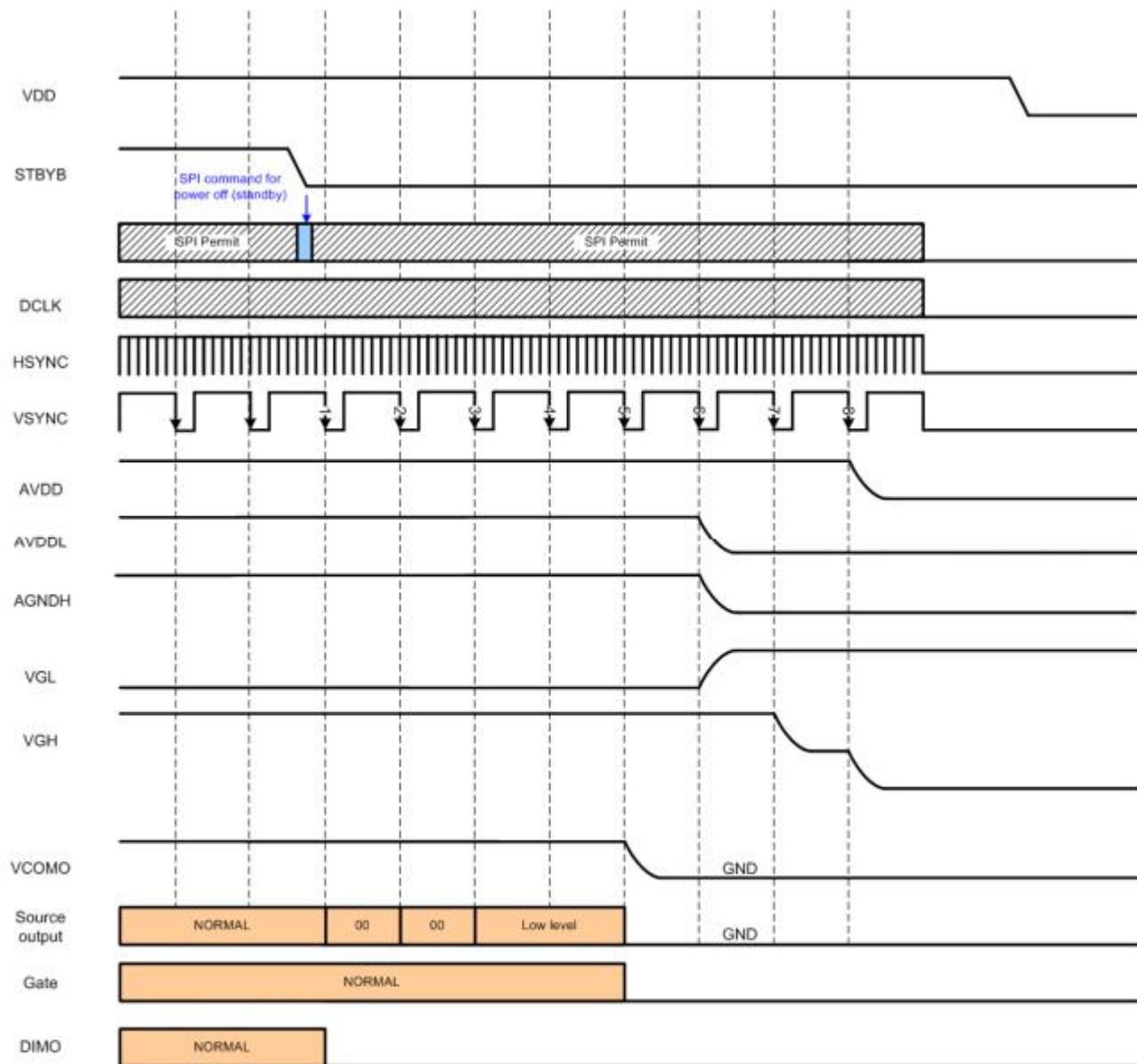


Figure 8.1: Power on timing sequence

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Power off timing sequenc



Note: (1) Low level=3FH, when NBW=L. (**Normally white**)
(2) Low level=00H, when NBW=H. (**Normally black**)

Figure 8.2: Power off timing sequence

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5.INPUT SIGNAL TIMING.

5.1 LVDS mode DC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Differential input high Threshold voltage	R_{XVTH}	-	-	+0.1	V	$R_{XVCM}=1.2V$
Differential input low threshold voltage	R_{XVTL}	-0.1	-	-	V	
Input voltage range (singled-end)	R_{XVIN}	0	-	$VDD-1.2+ V_{ID} /2$	V	-
Differential input common Mode voltage	R_{XVCM}	$ V_{ID} /2$	-	$VDD-1.2$	V	-
Differential input voltage	$ V_{ID} $	0.2	-	0.6	V	-
Differential input leakage Current	RV_{Xliz}	-10	-	+10	μA	-
LVDS Digital Operating Current	$Iddlvds$	-	15	30	mA	$Fclk=65MHz, VDD=3.3V$
LVDS Digital Stand-by Current	$Istlvds$	-	10	50	μA	Clock & all Functions are stopped

Table 9.3: LVDS mode DC electrical characteristics

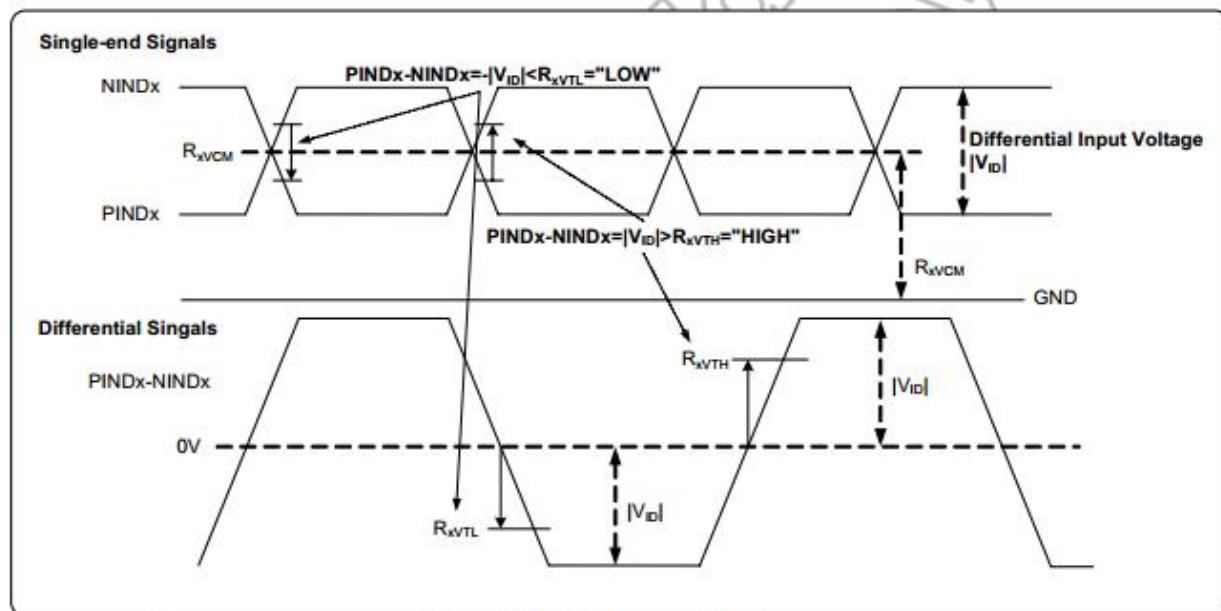


Figure 9.1: Single-end signals

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5.2 AC CHARACTERISTICS

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{XFCLK}	20	-	71	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	pS	$ V_{ID} =400mV$ $R_{XVCM}=1.2V$ $R_{XFCLK}=71MHz$
Clock high time	T_{LVCH}	-	$4/(7 \cdot R_{XFCLK})$	-	ns	-
Clock low time	T_{LVCL}	-	$3/(7 \cdot R_{XFCLK})$	-	ns	-
PLL wake-up time	T_{emPLL}	-	-	150	μs	-

Table 10.2: LVDS mode AC electrical characteristics

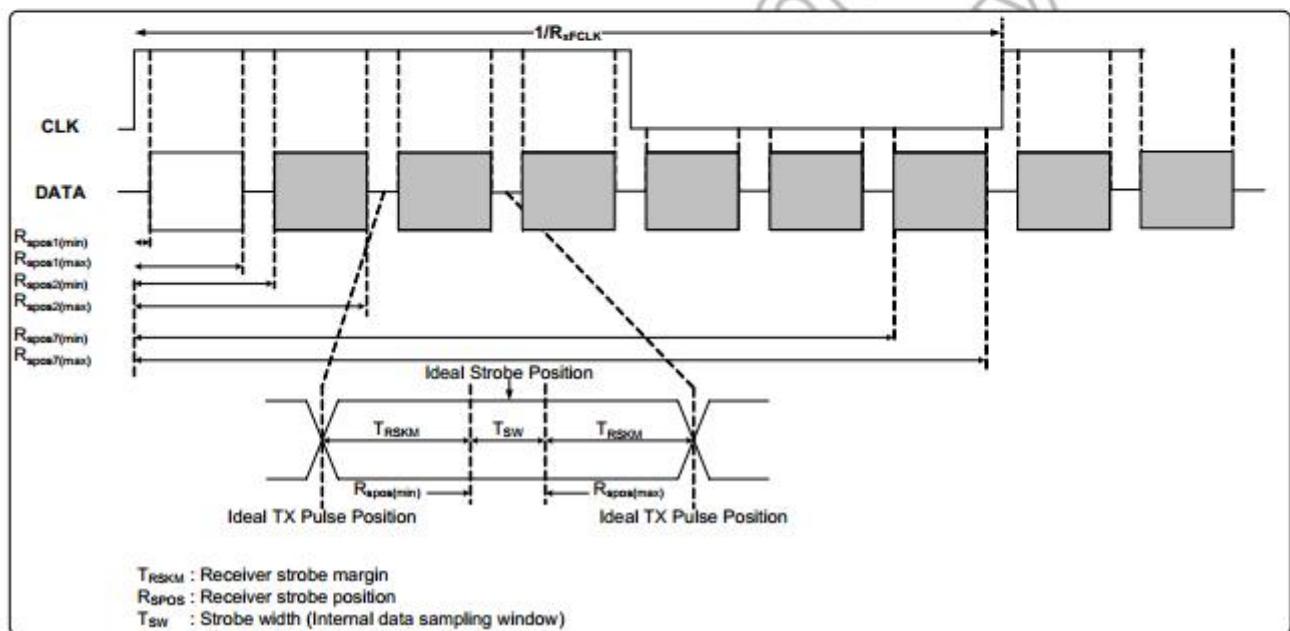
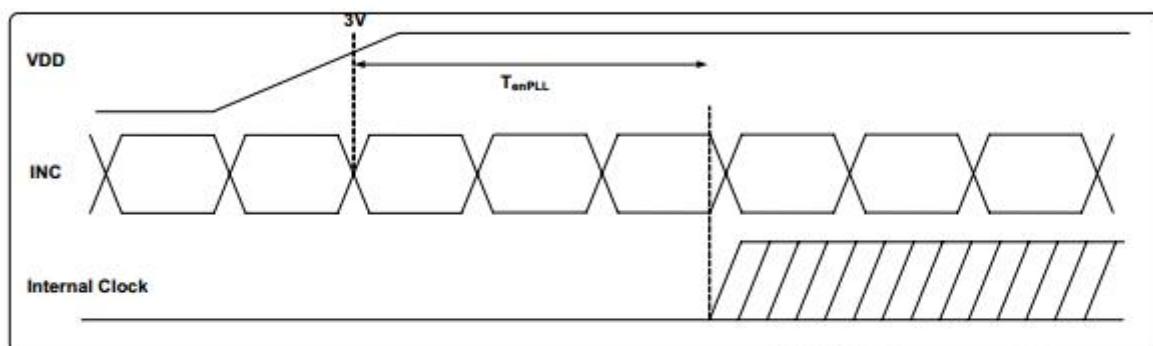
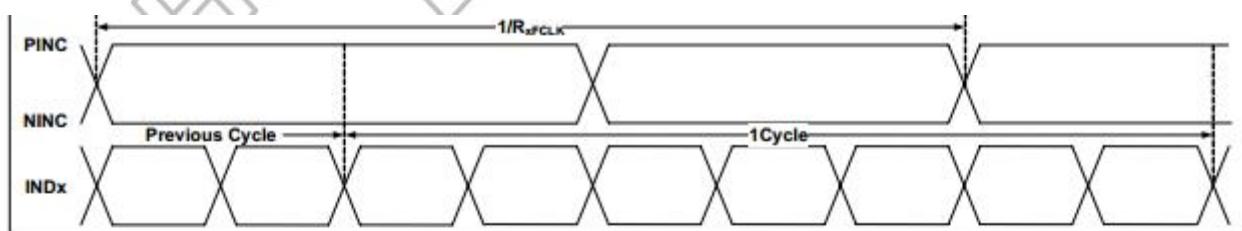
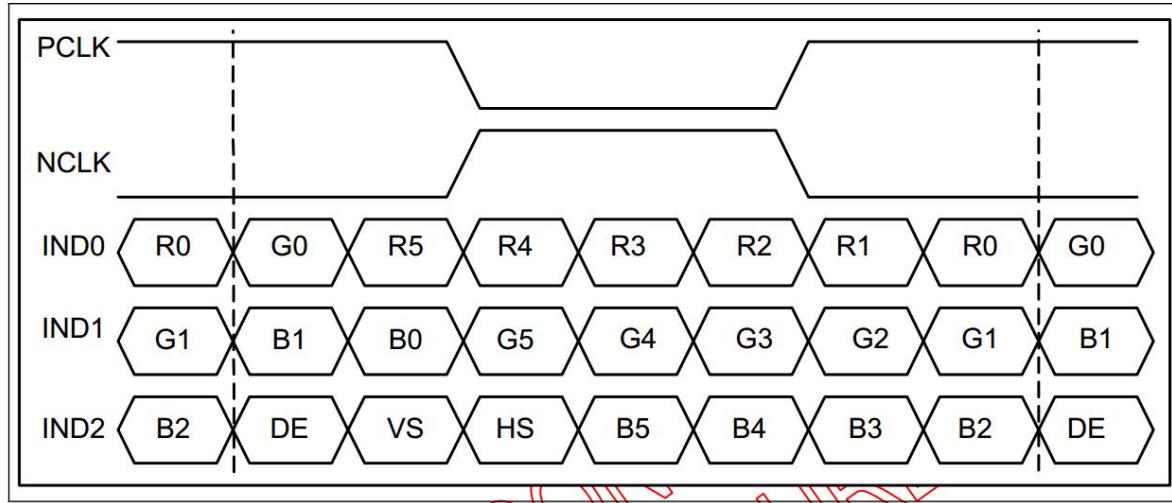


Figure 10.1: LVDS figure

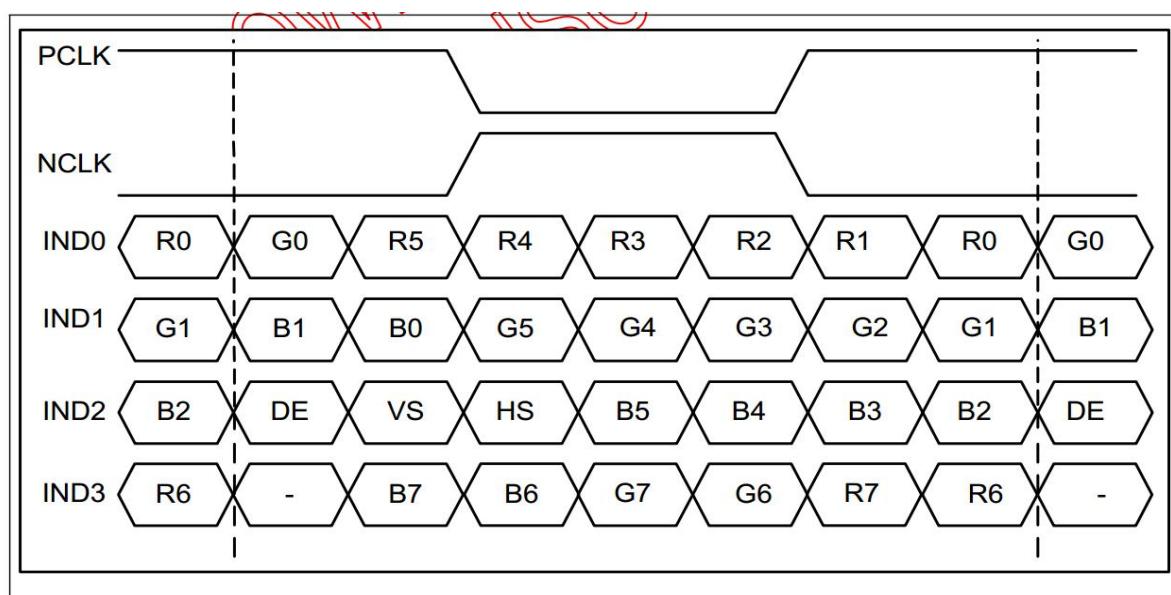
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5.3 Bit LVDS INPUT

5.3.1 6bit LVDS input (SELB="1")



5.3.1 8BIT LVDS INPUT (SELB="0")



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5.4 INTERFACE TIMING

DE MODE

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd		600		T _H
VSD Period	tv	610	635	800	T _H
VSD Blanking	tvbp+ tvfp	10	35	200	T _H

Table 10.4: DE mode (1024x600)

HV mode

Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp		160		DCLK
HSD Front Porch	thfp	16	160	216	DCLK

Table 10.5: HV mode horizontal timing (1024x600)

Vertical Timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		T _H
VSD Period	tv	624	635	750	T _H
VSD Pulse Width	tvpw	1	-	20	T _H
VSD Back Porch	tvbp		23		T _H
VSD Front Porch	tvfp	1	12	127	T _H

Table 10.6: HV Mode Vertical Timing (1024x600)

Parallel 24-bit RGB mode

Parameter	Symbol	Spec.			Unit	Conditions
		Min.	Typ.	Max.		
CLKIN Frequency	Fclk	-	65	71	MHz	VDD=3.0V~3.6V
CLKIN Cycle Time	Tclk	14.1	15.4	-	ns	-
CLKIN Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso		64		CLKIN	-
Time from HSD to LD	Thld		64		CLKIN	-
Time from HSD to STV	Thstv		2		CLKIN	-
Time from HSD to CKV	Thckv		20		CLKIN	-
Time from HSD to OEV	Thoev		4		CLKIN	-
LD Pulse Width	Twld		10		CLKIN	-
CKV Pulse Width	Twckv		66		CLKIN	-
OEV Pulse Width	Twoev		74		CLKIN	-

Table 11.1: Parallel 24-bit RGB mode

11.2.1 Input clock and data timing diagram

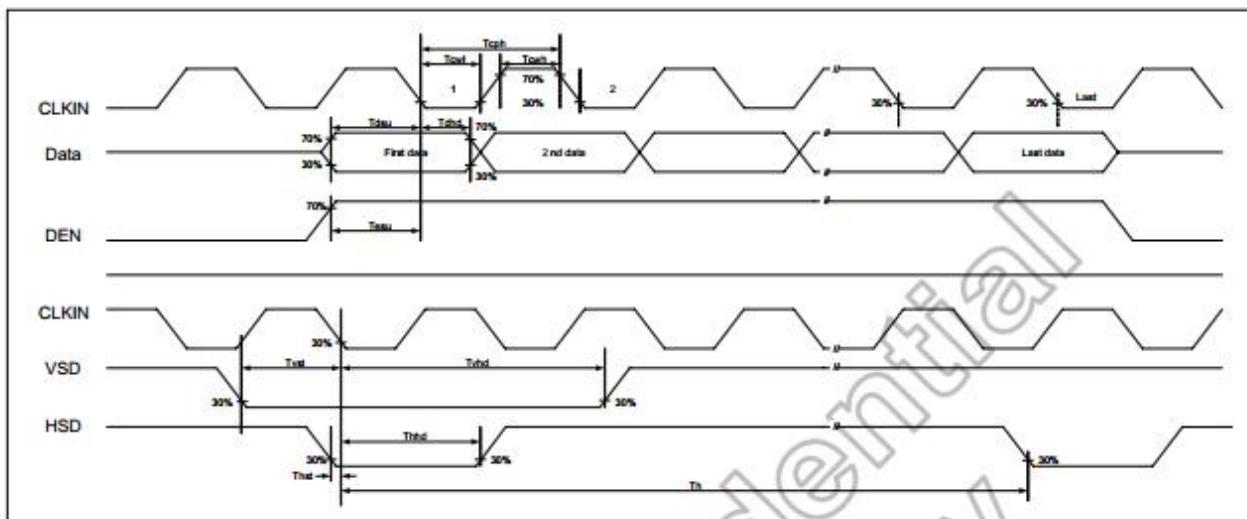


Figure 11.1: Input clock and data timing diagram

11.2.2 Source output timing diagram (Cascade)

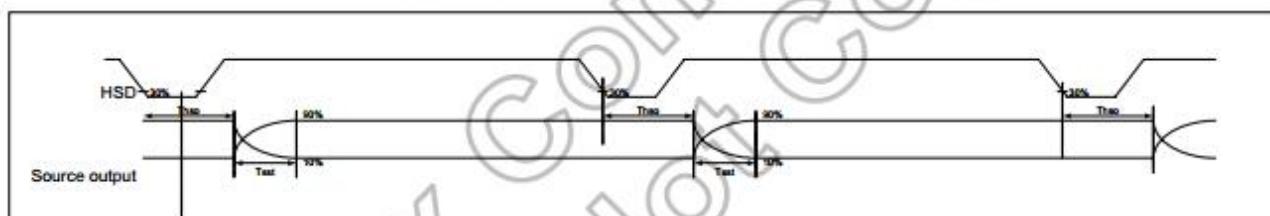


Figure 11.2: Source output timing diagram

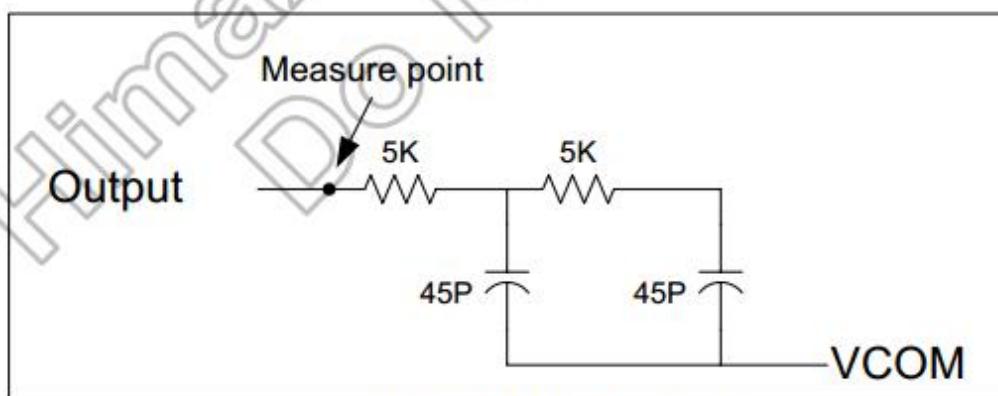


Figure 11.3: Output load condition

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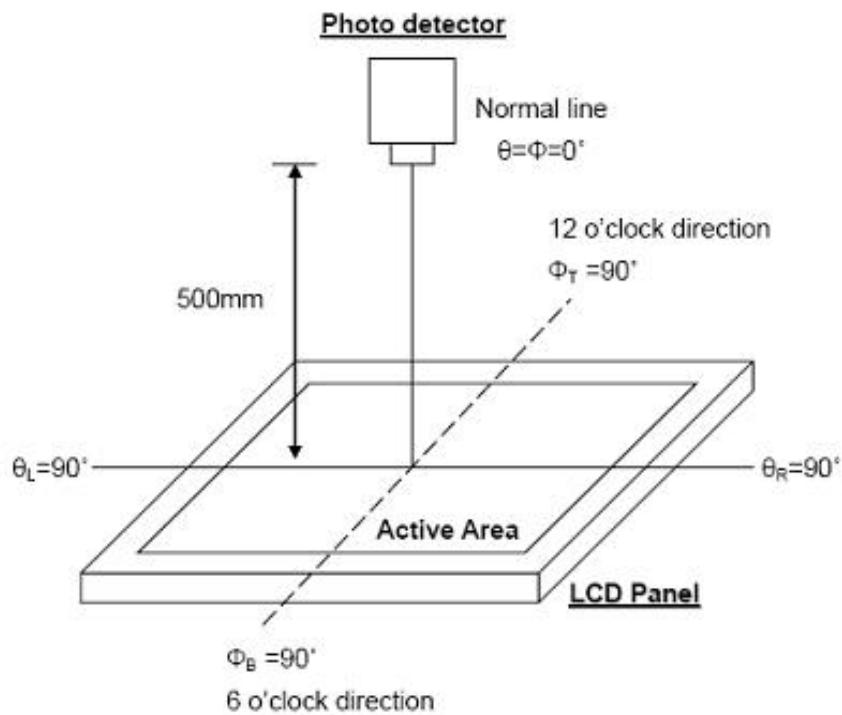
6.OPTICAL CHARACTERISTICS

T_a=25±2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Contrast Ratio	CR	-	800	-		Note1 Note3
Luminance(center)	L	400	450	-	cd/m ²	Note1 Note5 Note7
Luminous tolerance	LU	70	75		%	Note7
Response Time	Rising + Falling	-	30	40	ms	Note1 Note4
Viewing Angle K=Contrast Ratio>10	Horizontal	θx ⁺		85	-	degree Note2
		θx ⁻		85	-	
	Vertical	θy ⁺		85	-	
		θy ⁻		85	-	
Color Chromaticity (CIE1931)	Red	x	Typ- 0.05	0.617	Typ+ 0.05	Note1 Note5 Note7
		y		0.327		
	Green	x		0.332		
		y		0.600		
	Blue	x		0.146		
		y		0.056		
	White	x		0.299		
		y		0.331		
Color gamut (NTSC ratio)			50		%	
Optima View Direction			free			

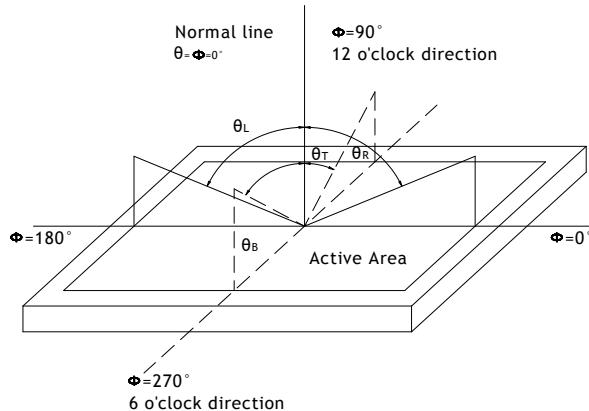
Note1: Definition of optical measurement system (BM-7)

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Note2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

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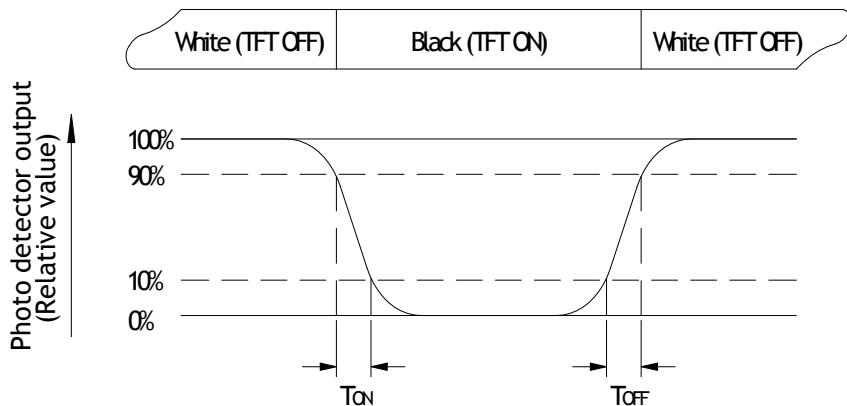


Fig. 6-3 Definition of response time

Note4: Definition of contrast ratio

Contrast ratio(CR)=错误！未找到引用源。

“White state”：The state is that the LCD should drive by Vwhite.

“Black state”：The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

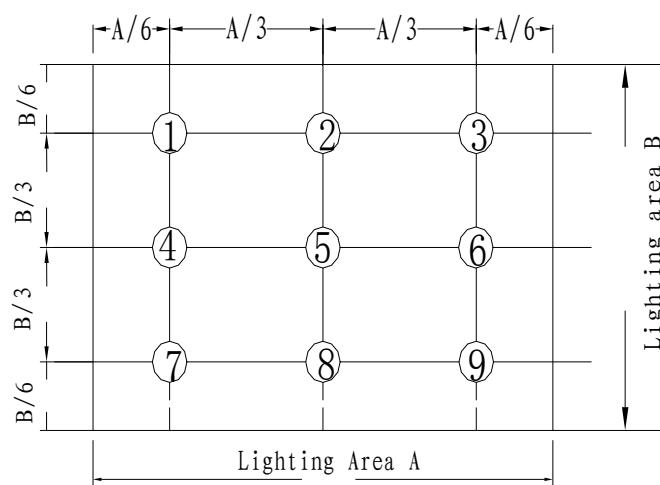
Note6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IL=180mA

Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas. Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = L_{min} / L_{max}

L----Active area length, W---- Active area width



B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

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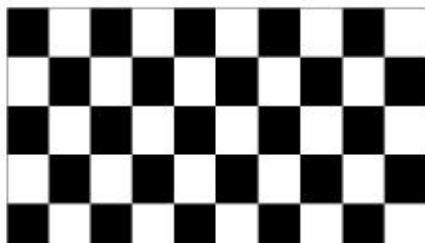
7.RELIABILITY TEST ITEMS

7.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition	Remark
High Temperature Storage	Ta=80°C; 12hrs	IEC60068-2-1: 2007 GB2423.2-2008
Low Temperature Storage	Ta=-30°C;12hrs	IEC60068-2-1: 2007 GB2423.1-2008
High Temperature Operation	Ta=70°C, 24Hrs	IEC60068-2-1: 2007 GB2423.2-2008
Low Temperature Operation	Ta=-20°C; 24hrs	IEC60068-2-1: 2007 GB2423.1-2008
High Temperature High Humidity Operation	Ta=50°C, 90%RH, 24Hrs(no condensation)	IEC60068-2-78: 2001 GB/T2423.3-2006
Thermal Shock	-30°C(0.5h) ~ 80°C(0.5h) / 50 cycles	Start with cold temperature , End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
Image Sticking	25°C ; 1hrs	Note1

Note1:Condition of image sticking test : $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$

Operation with test pattern sustained for 1hrs,then change to gray pattern immediately.after 15 mins,the mura must be disappeared completely



(a) Test Pattern (chess board Pattern)



(b) Gray Pattern

7.2 VIBRATION&SHOCK

Test item	Conditions	Remark	
Packing Shock (non-operation)	980m/s ² ,6ms, ±x,y,z 3times for direction	IEC60068-2-27: 1987 GB/T2423.5-1995	
Packing Vibration (non-operation)	Frequency range:10 HZ~50HZ Stroke:1.0mm,sweep:10 HZ ~50HZ x,y,z 2 hours for each direction	IEC60068-2-32: 1990 GB/T2423.8-1995	

7.3 ESD

Test item	Conditions	Remark	
Electro Static Discharge Test (non-operation)	150pF, 330Ω, Contact: $\pm 2\text{KV}$,Air: $\pm 4\text{KV}$	1	Class C
	200pF, 0Ω, $\pm 200\text{V}$ contact test	2	

Note: Measure point :

1. LCD glass and metal bezel
2. IF connector pins
3. ESD class C: To allow a temporary loss of function, the equipment to be measured may stop working but should be able to automatic or manual intervention reset back to normal after

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operation.

8. GENERAL PRECAUTION

8.1 SAFETY

1. Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
2. If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
3. If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

1. Store the panel or module in a dark place where the temperature is $23 \pm 5^\circ \text{C}$ and The humidity is below $50 \pm 20\% \text{RH}$.
2. Store in anti-static electricity container.
3. Store in clean environment, free from dust, active gas, and solvent.
4. Do not place the module near organics solvents or corrosive gases.
5. Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

1. Avoid static electricity which can damage the CMOS LSI.
2. The polarizing plate of the display is very fragile. So, please handle it very carefully.
3. Do not give external shock.
4. Do not apply excessive force on the surface.
5. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the Surface of plate.
6. Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
7. Do not operate it above the absolute maximum rating.
8. Do not remove the panel or frame from the module.
9. When the module is assembled, it should be attached to the system firmly, Be careful not to twist and bend the module.
10. Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.
11. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth in case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

8.4 WARRANTY

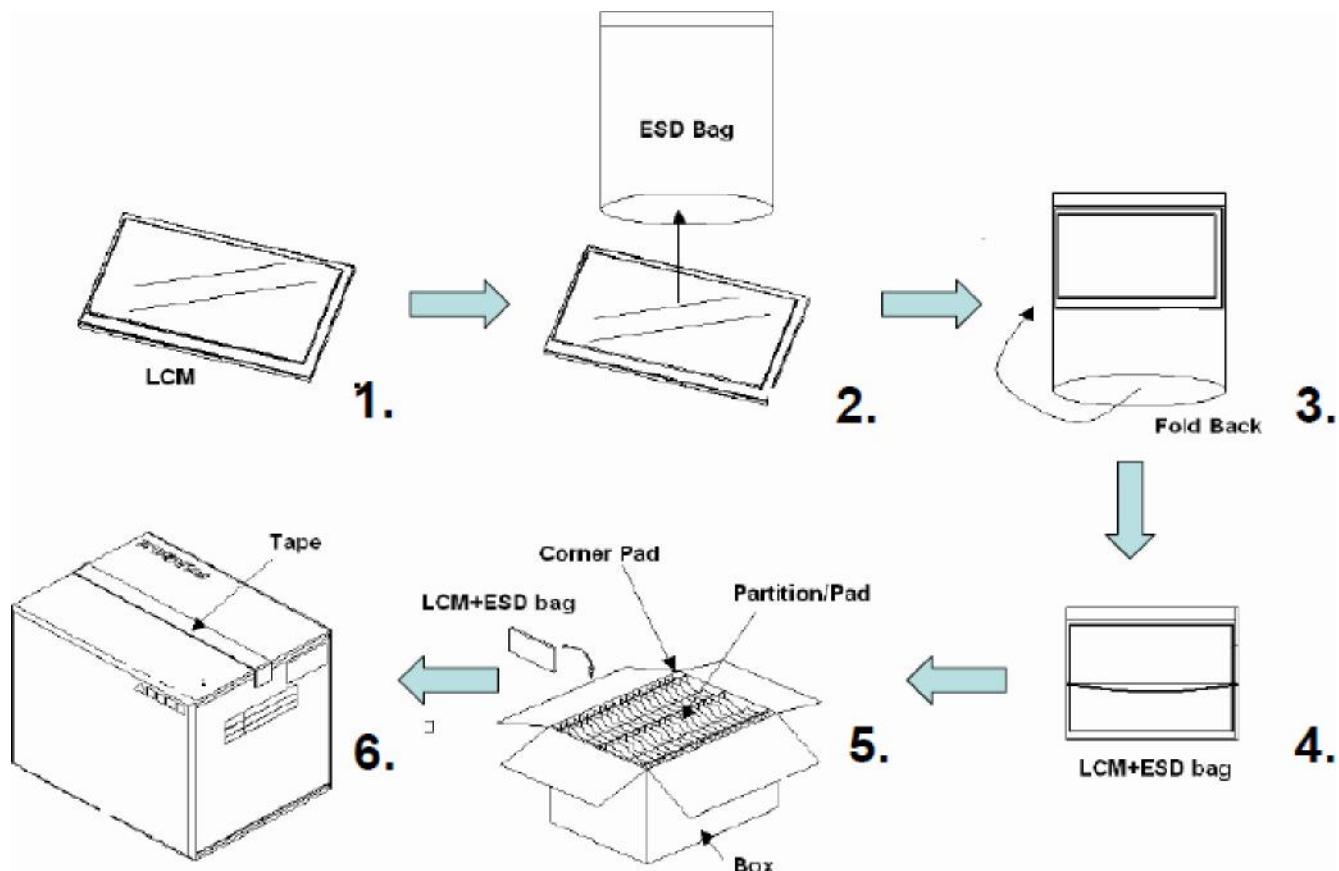
1. The period is within twelve months since the date of shipping out under normal using and storage conditions.
2. Do not repaired or modified the LCM. It may cause function to lose efficacy, Starry does not warrant the LCM.
3. All process and material comply ROHS.

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9. PACKAGE DRAWING

Packing form

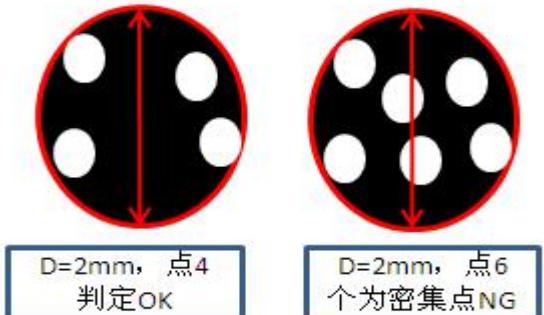
LCM Model	LCM Qty. in the box	Inner Box Size (mm)	Notice
	50 pcs/box	455±5 x 305±5 x 205±5	



Items	Material	Notice
Box	Corrugated Paper Board	AB Flute
Partition/Pad	Corrugated Paper Board	B Flute
Corner Pad	Corrugated Paper Board	AB Flute
ESD bag	PE	

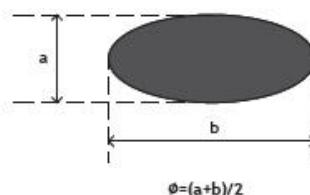
INCOMING INSPECTION STANDARDS

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	Dense point	Using ND5 % visible by intensive foreign standard judgement, ND5 % invisible OK	Note 4
			

- (1) One pixel consists of 3 sub-pixel, including r,g,ang b dot.(sub-pixel=dot)
(2) Panel is acceptable if distance between 2 dot defects are greater or equal to 5mm.

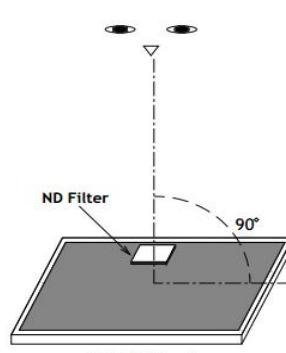
Note1 : W : Width[mm], L : Length[mm], N : Number, ϕ : Average Diameter



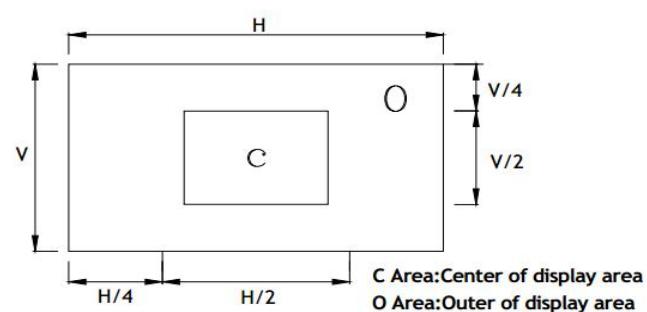
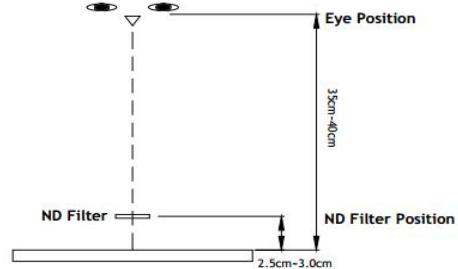
1.(White ,Black) Spot
2.Polarizer Bubble



Scratch & Fiber



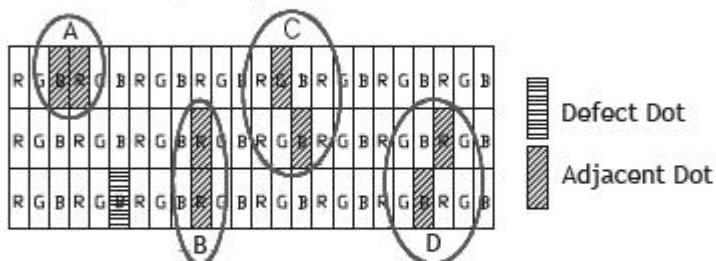
Note3 :



C Area:Center of display area
O Area:Outer of display area

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Note4 : Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dark adjacent dot. And they will be counted 2defect dots in total quantity.



Note5 : Other condition

- (1) The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.
- (2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

5. HANDLING PRECAUTION

- (1) Don't disassemble and reassemble the module by self
(禁止自行拆解)
- (2) Acid, alkali, alcohol or touched directly by hand will damage the display.
(酸性、碱性、酒精或手的直接接触将会损伤显示面)
- (3) Static electricity will damage the module. Please configure grounding device.
(静电会损伤模组, 请装配接地设备)
- (4) The strong vibration, shock, twist or bend will cause material damage, even module broken.
(强烈的撞击、震动、扭转或弯曲将会造成原材损伤, 甚至面板破裂)
- (5) It is easy to cause image sticking while displaying the same pattern for very long time.
(长期显示同一画面会造成影像残留)
- (6) The response time, brightness and performance will vary from different temperature.
(响应时间、亮度与均匀性会因温度而有所改变)
- (7) The Period within 12 months since the date of shipping out under normal using And Storage conditions.
(从出货之日起开始,在正常使用和存储条件下,产品保质期为12个月)